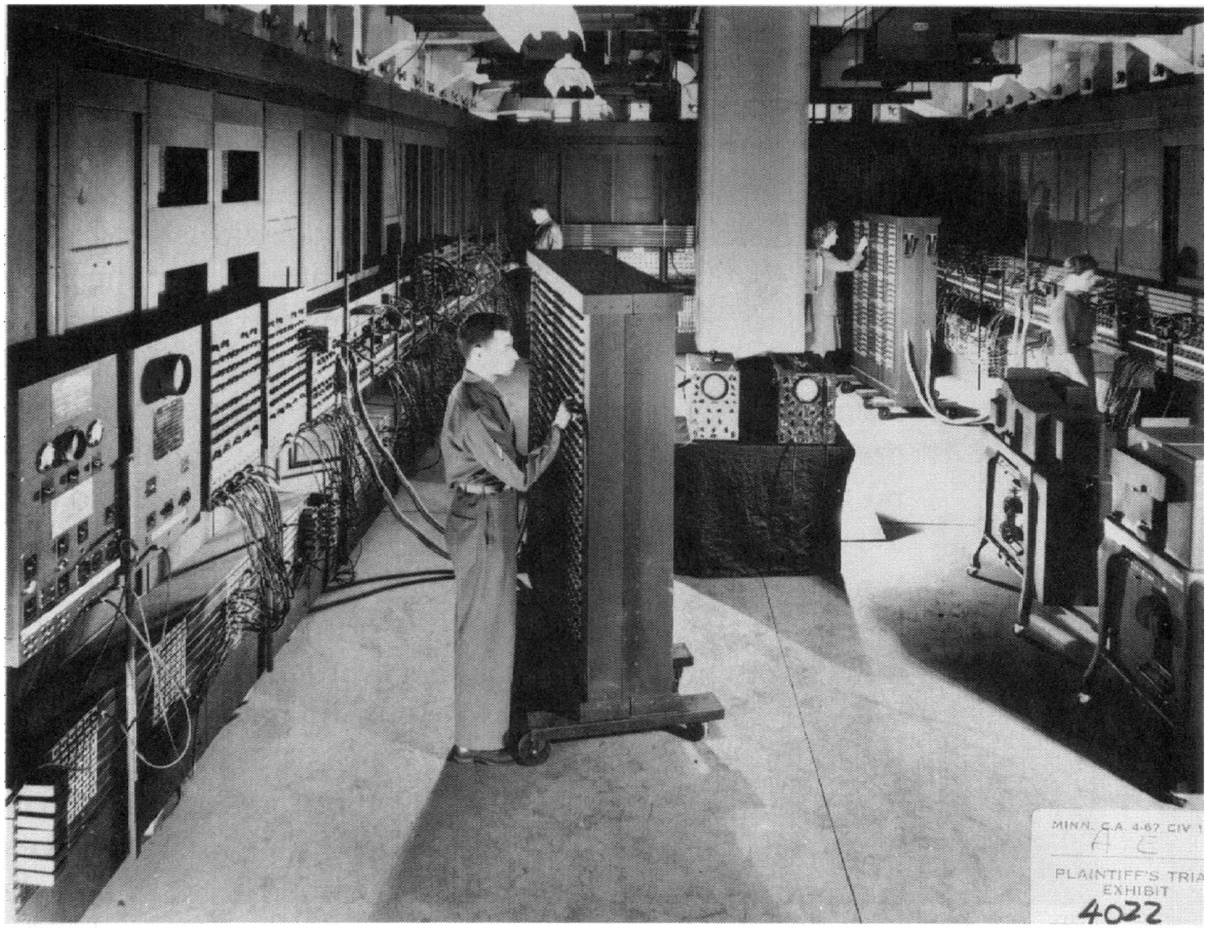
An Introduction to VLSI (Very Large Scale Integrated) Circuit Design

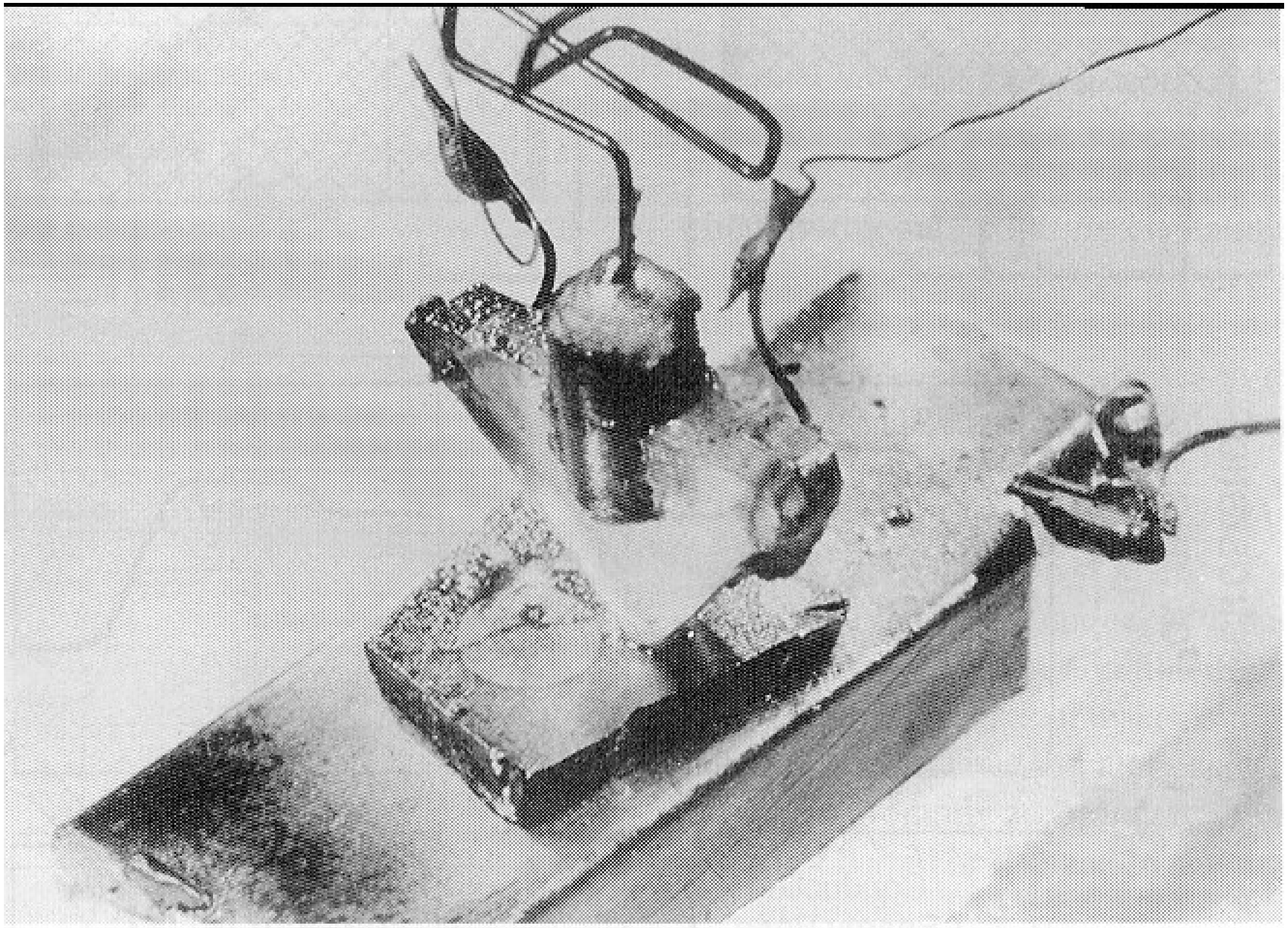
Presented at EE1001
Oct. 16th, 2018

By Hua Tang

The first electronic computer (1946)

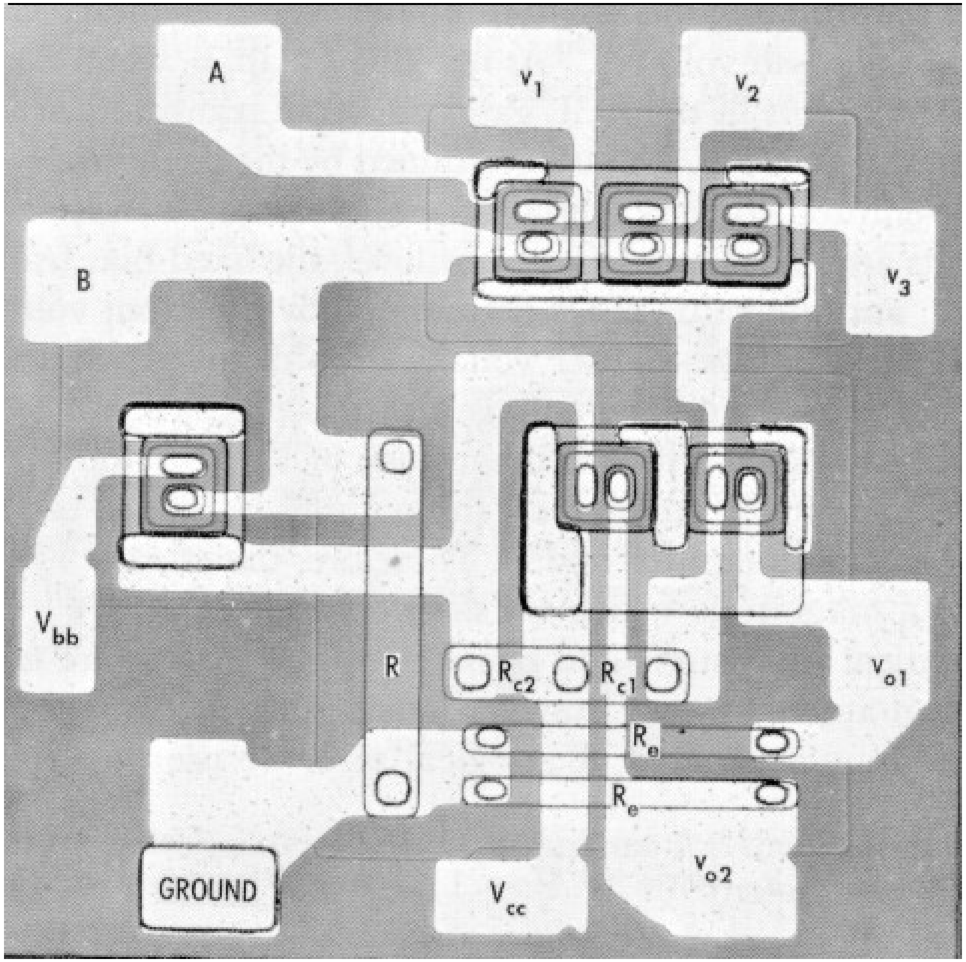


First Transistor (Bipolar)



First transistor
Bell Labs, 1948

The First Integrated Circuits

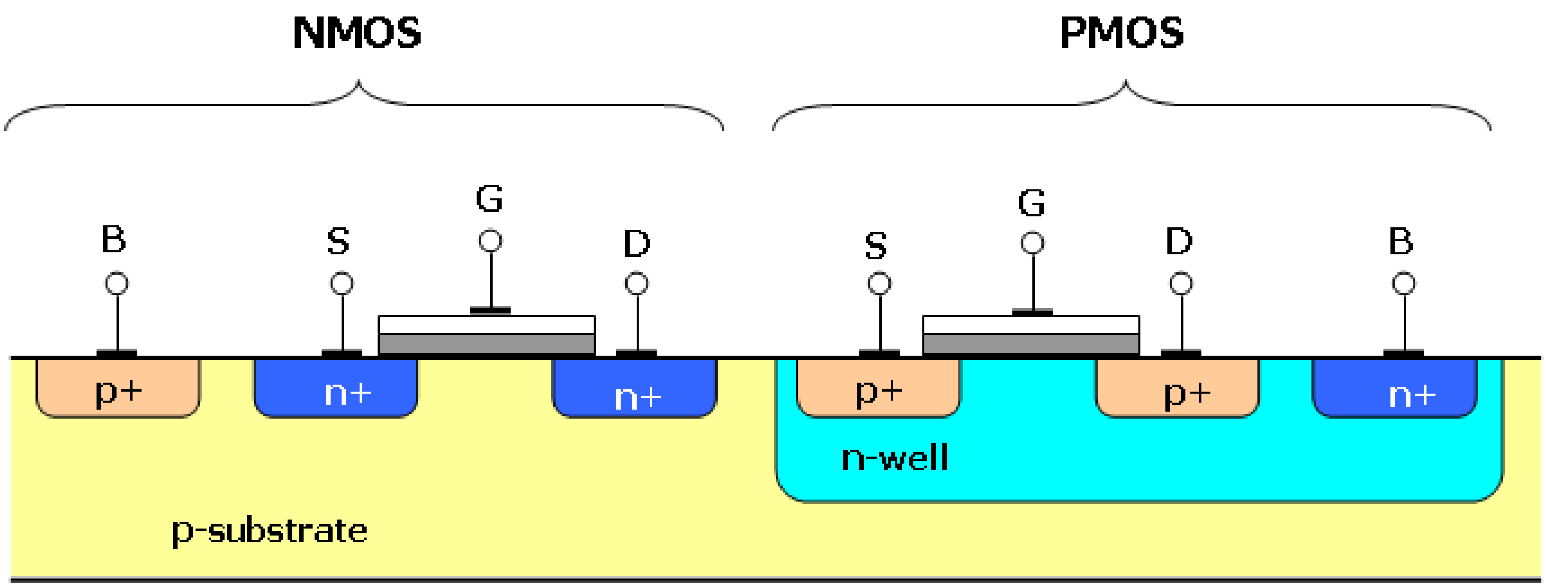


Bipolar logic
1960's

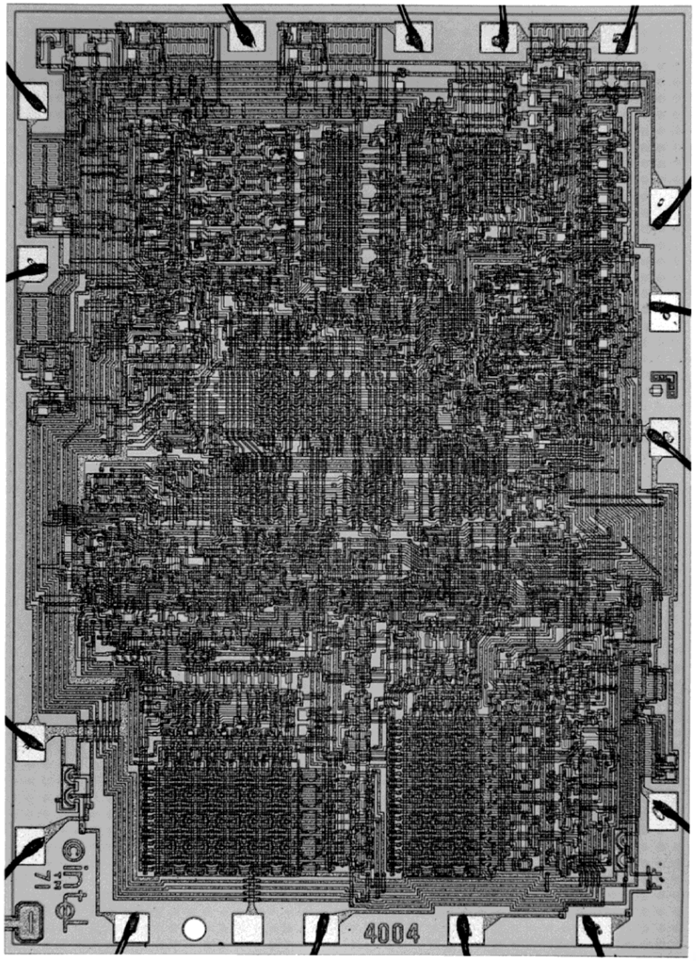
ECL 3-input Gate
Motorola 1966

Basic IC circuit component: MOS transistor

MOS: Metal Oxide Semiconductor

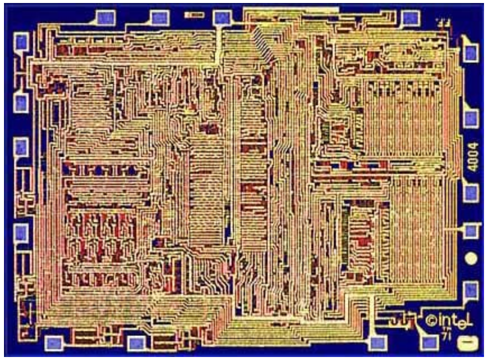


Intel 4004 Micro-Processor

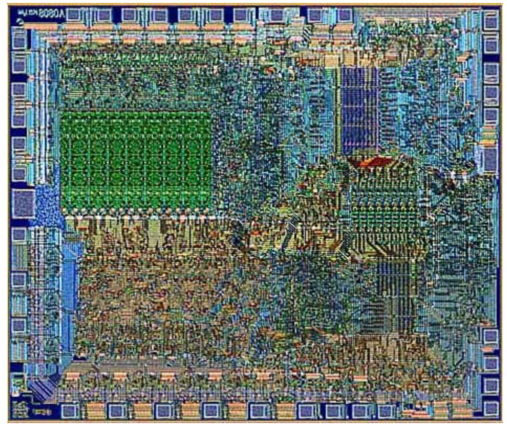


1971
1000 transistors
< 1MHz operation
10μm technology

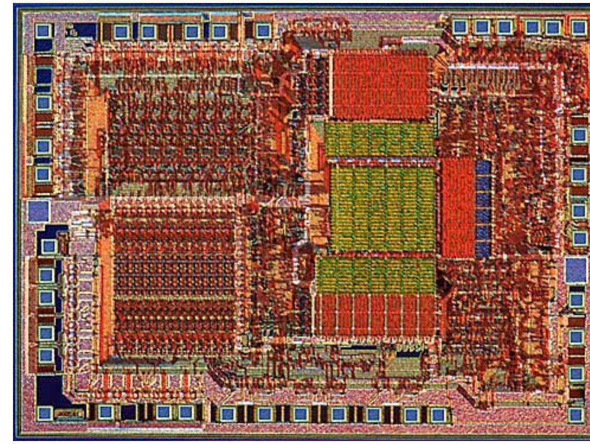
Transition to Automation and Regular Structures



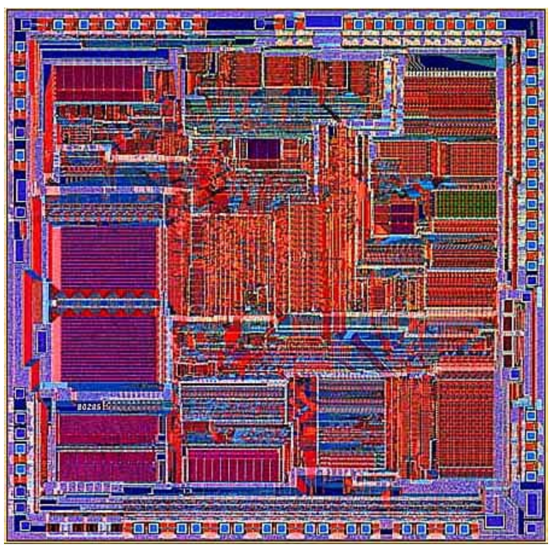
Intel 4004 ('71)



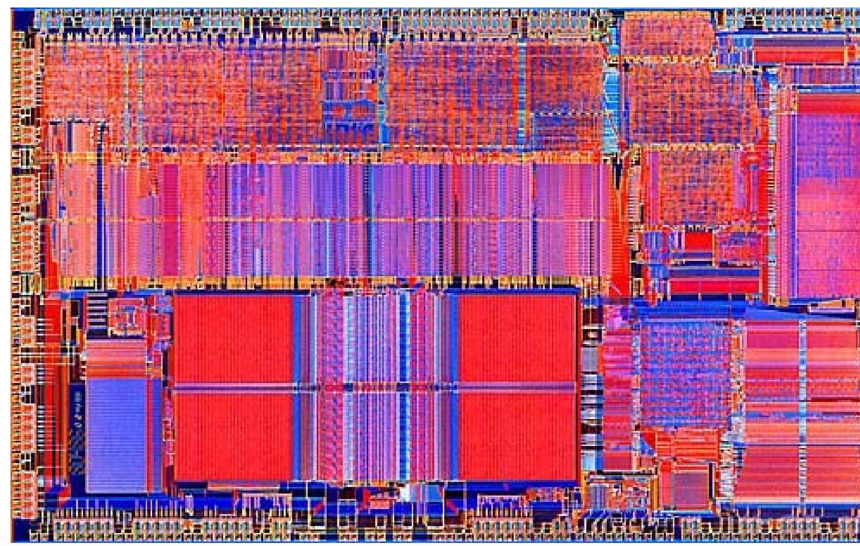
Intel 8080



Intel 8085



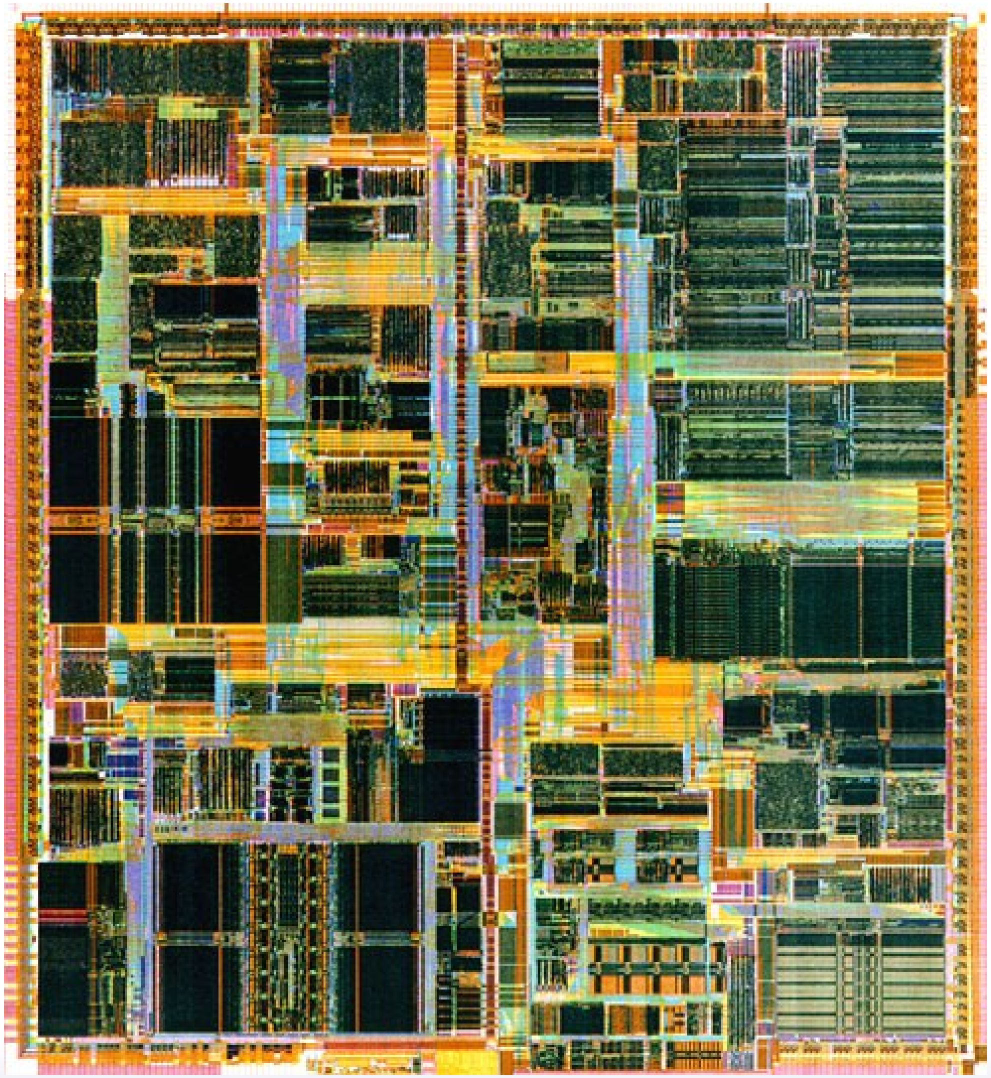
Intel 8286



Intel 8486

Courtesy Intel

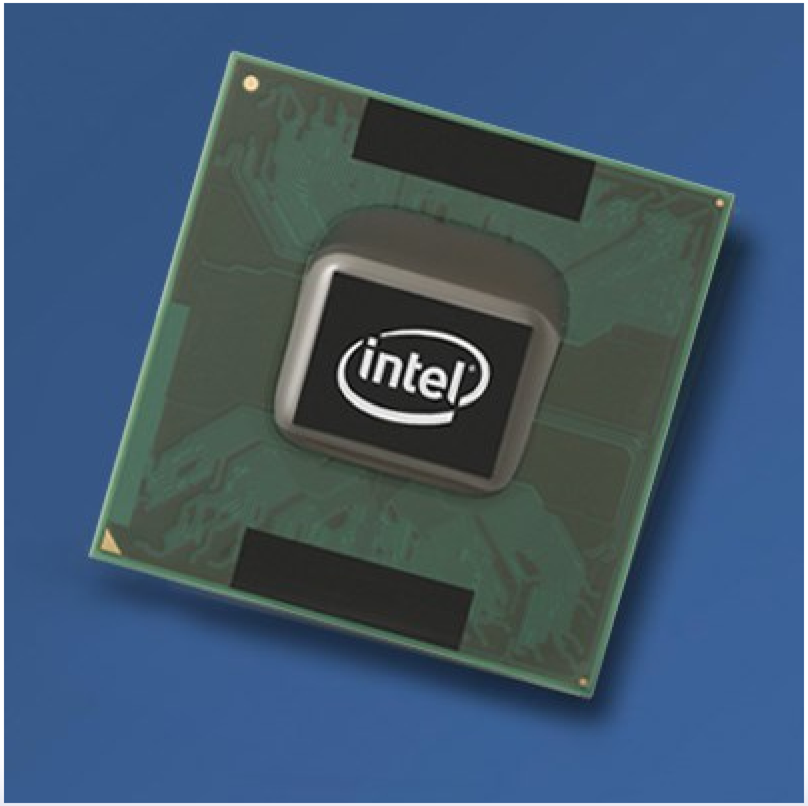
Intel Pentium (IV) microprocessor



2001
42 Million transistors
1.5 GHz operation
0.18μm technology

Intel Core™ 2 Duo Processor

2006
291 Million transistors
3 GHz operation
65nm technology



More recent Processors

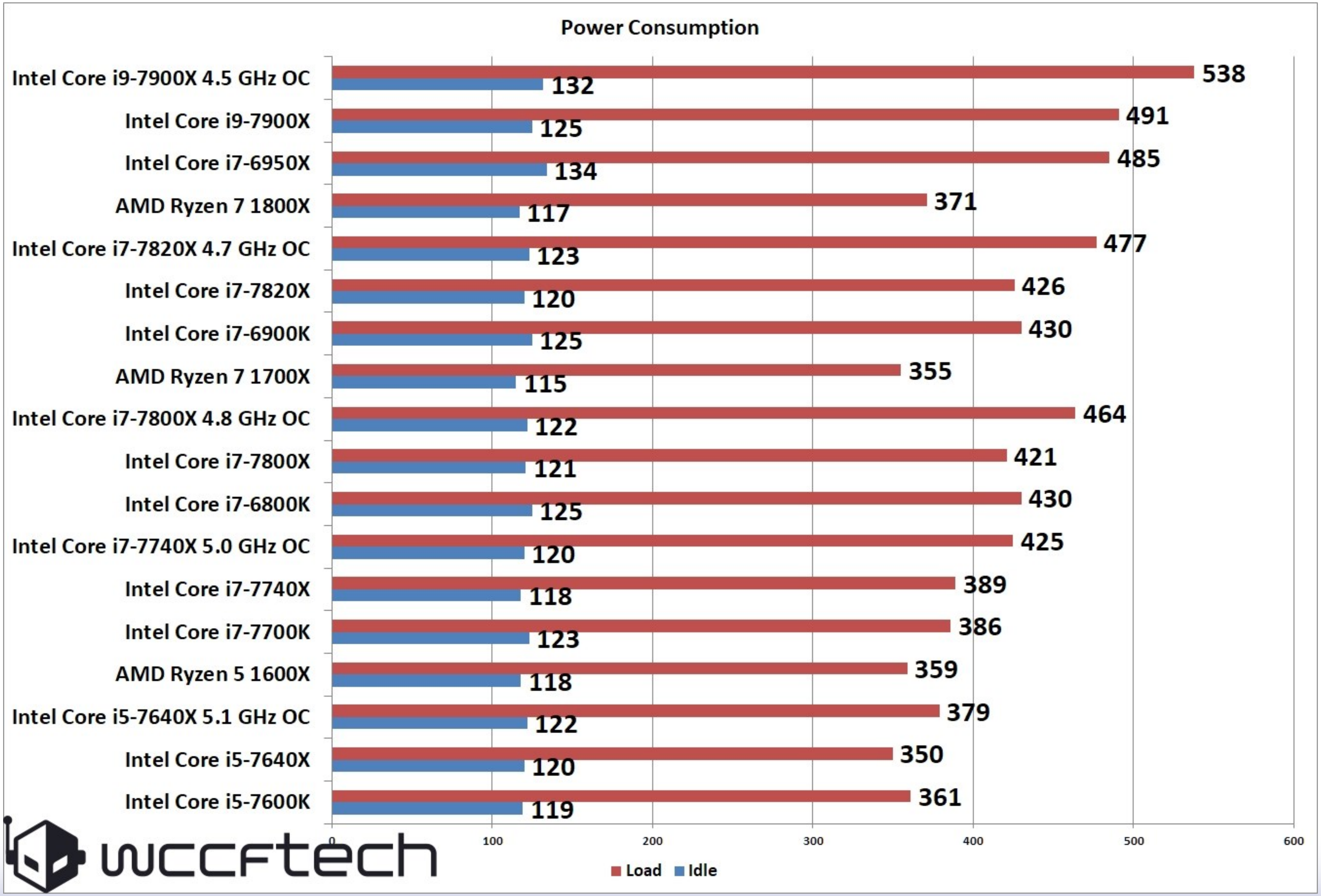
- 2007
  - 800 Million transistors
  - 2 GHz operation
  - 45nm technology
- 2010 Core i7
  - 1.2 Billion transistors
  - 3.3 GHz operation
  - 32nm technology
- 2012 Core i7 (newer generations)
  - 1.7 Billion transistors
  - 4.0 GHz operation
  - 22nm technology
- 2015 14nm, 2017 10nm, and 2018 7nm, 2019 5nm?

More recent Processors

Apple A11 Bionic (hexa-core ARM64 "mobile SoC")	4,300,000,000	2017	Apple	10 nm	89 mm²
15-core Xeon Ivy Bridge-EX	4,310,000,000[36]	2014	Intel	22 nm	541 mm²
8-core Ryzen	4,800,000,000[37]	2017	AMD	14 nm	192 mm²
61-core Xeon Phi	5,000,000,000[38]	2012	Intel	22 nm	720 mm²
Xbox One main SoC	5,000,000,000	2013	Microsoft/AMD	28 nm	363 mm²
18-core Xeon Haswell-E5	5,560,000,000[39]	2014	Intel	22 nm	661 mm²
IBM z14	6,100,000,000	2017	IBM	14 nm	696 mm²
Xbox One X (Project Scorpio) main SoC	7,000,000,000[40]	2017	Microsoft/AMD	16 nm	360 mm²[40]
IBM z13 Storage Controller	7,100,000,000	2015	IBM	22 nm	678 mm²
22-core Xeon Broadwell-E5	7,200,000,000[41]	2016	Intel	14 nm	456 mm²
POWER9	8,000,000,000	2017	IBM	14 nm	695 mm²
72-core Xeon Phi	8,000,000,000	2016	Intel	14 nm	683 mm²
IBM z14 Storage Controller	9,700,000,000	2017	IBM	14 nm	696 mm²
32-core SPARC M7	10,000,000,000[42]	2015	Oracle	20 nm	
Centriq 2400	18,000,000,000[43]	2017	Qualcomm	10 nm	398 mm^2
32-core AMD Epyc	19,200,000,000	2017	AMD	14 nm	768 mm^2 (4 x 192 mm^2)

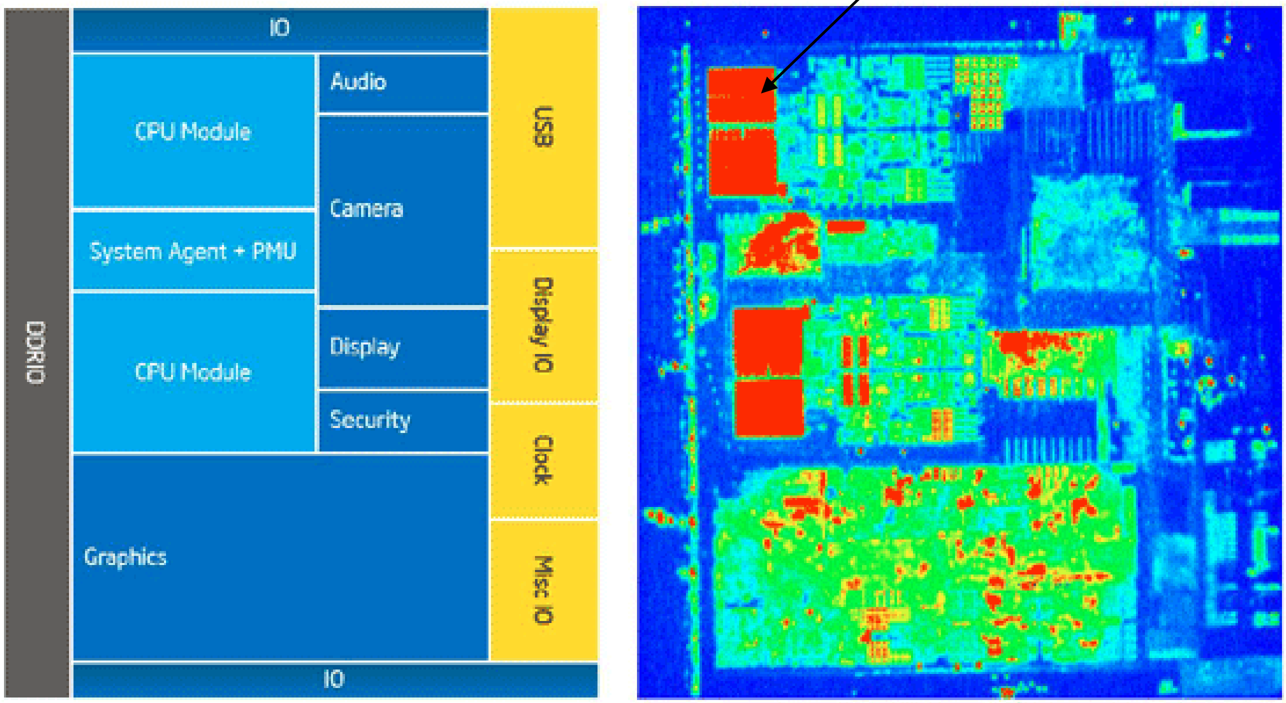
Source: https://en.wikipedia.org/wiki/Transistor_count

Power Consumption



Power density

Thermal hot spots



1. Hot spots are smaller in relation to the total die size
2. Scaling typically do NOT reduce power more than they reduce size (say from 90 nm -> 14 nm)
3. multi-core? Lowpower technologies?

Source: https://forums.anandtech.com/threads/cpu-power-density-trend.2416388/

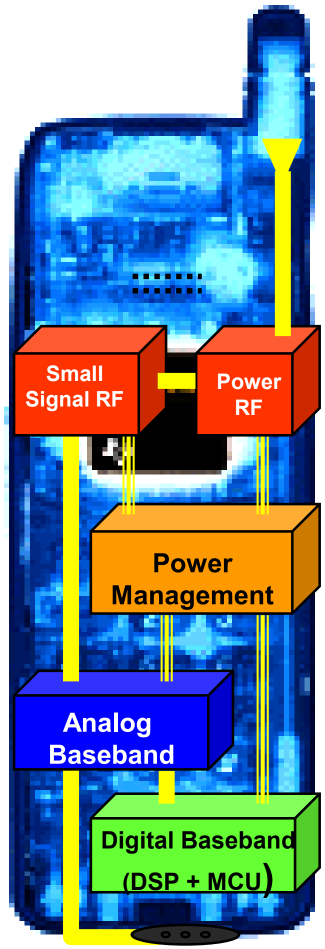
Not Only Microprocessors

Cell Phone

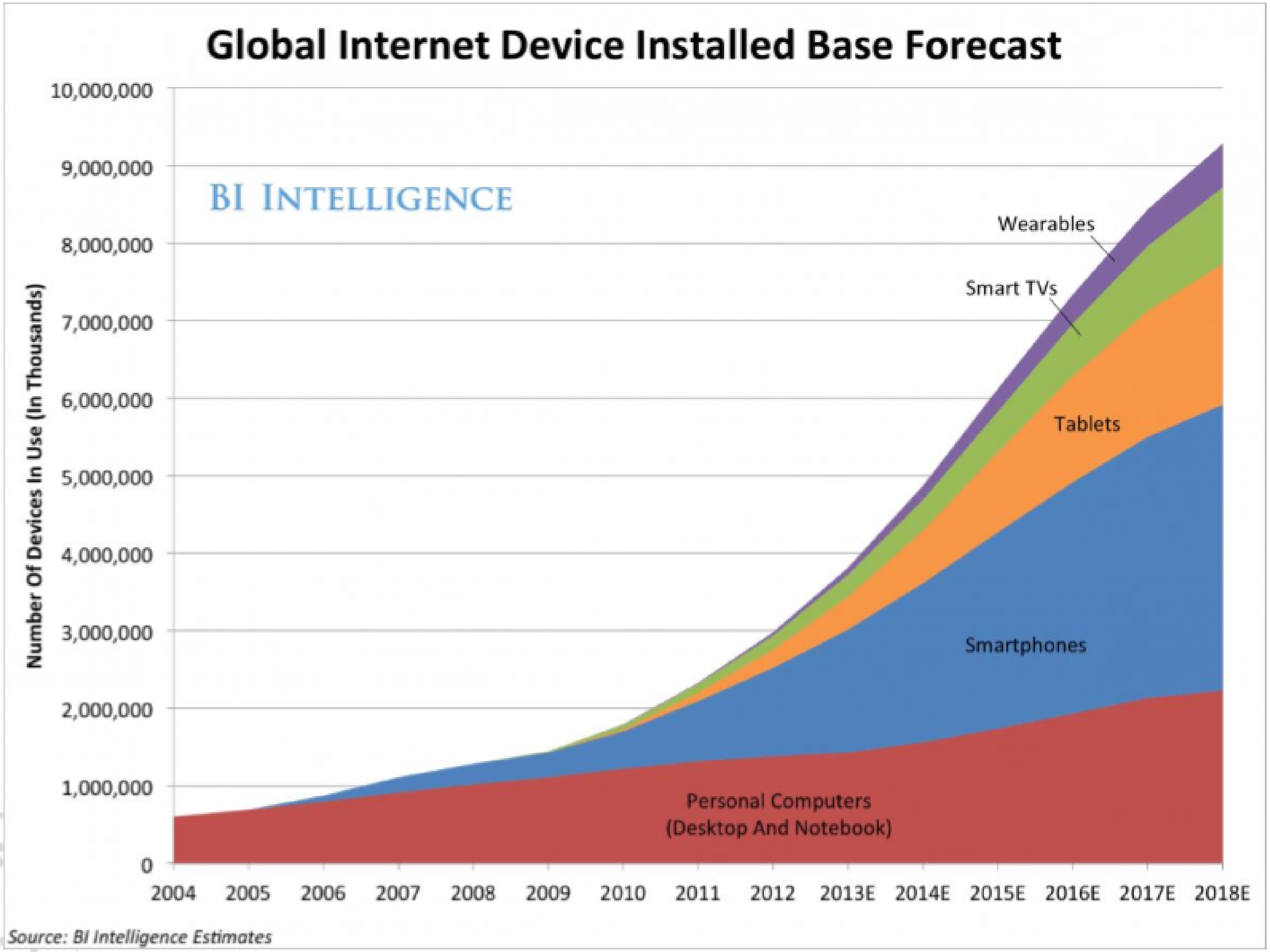
HDTV

PDA

….



Booming Mobile and IoT Applications

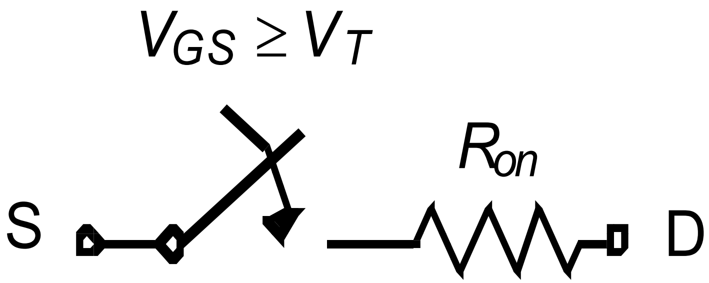


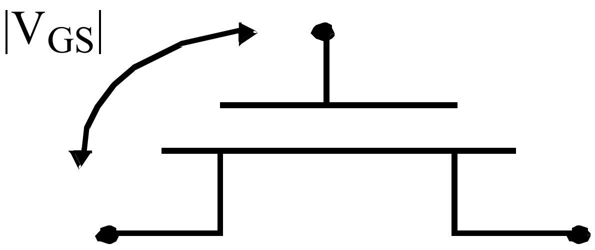
Source: An Chen, ConFab 2015

What is a MOS Transistor?

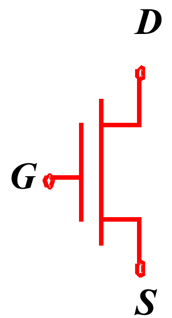
A Switch!

An MOS Transistor



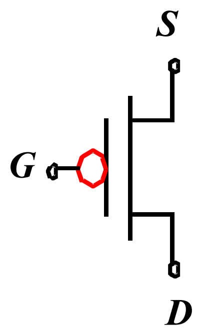


MOS Transistors - Types and Symbols



NMOS

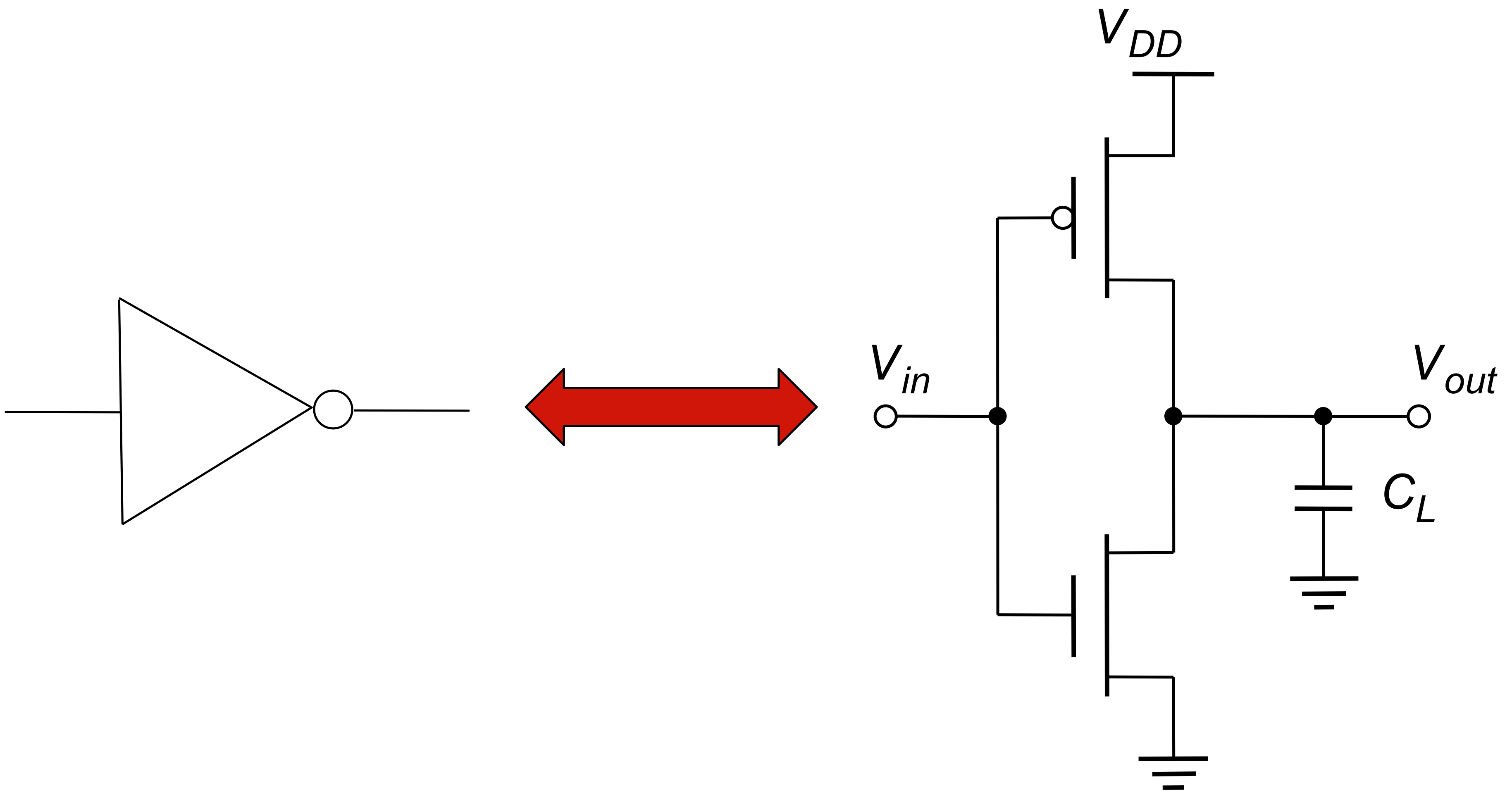
if *G*="1" or Vdd
switch on



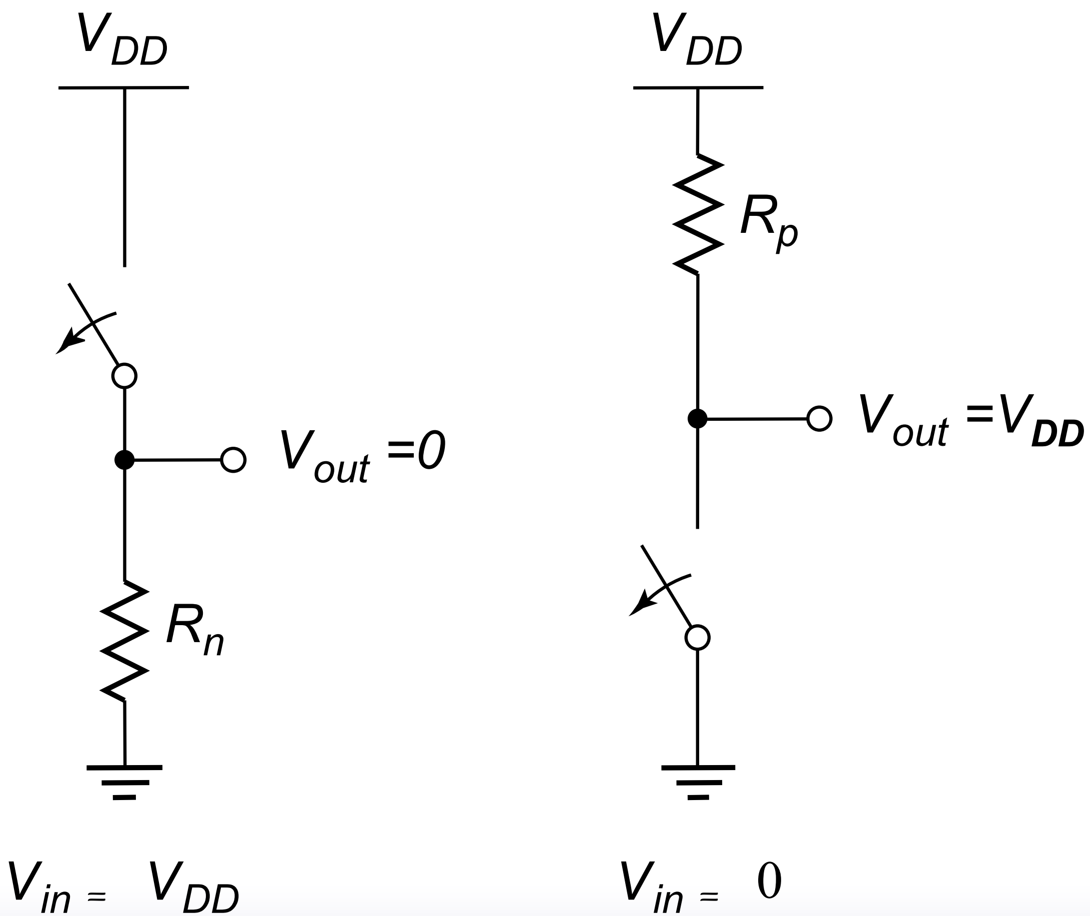
PMOS

if *G*="0" or Gnd
switch on

The CMOS Inverter: A First Glance



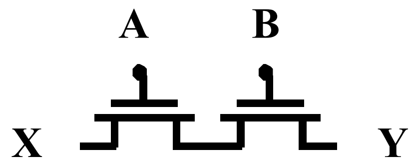
CMOS Inverter
First-Order DC Analysis



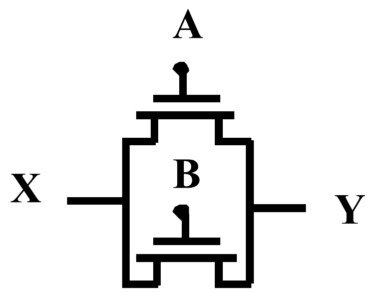
NMOS Transistors in Series/Parallel Connection

Transistors can be thought as a switch controlled by its gate signal

NMOS switch closes when switch control input is high



Y = X if A and B

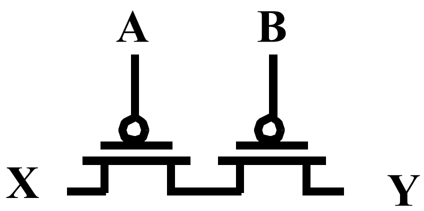


Y = X if A OR B

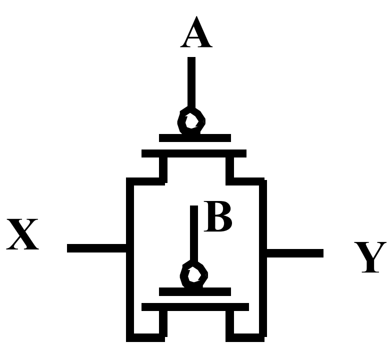
NMOS Transistors pass a “strong” 0 but a “weak” 1

PMOS Transistors in Series/Parallel Connection

PMOS switch closes when switch control input is low



$Y = X$ if $\overline{A}$ AND $\overline{B} = \overline{A + B}$



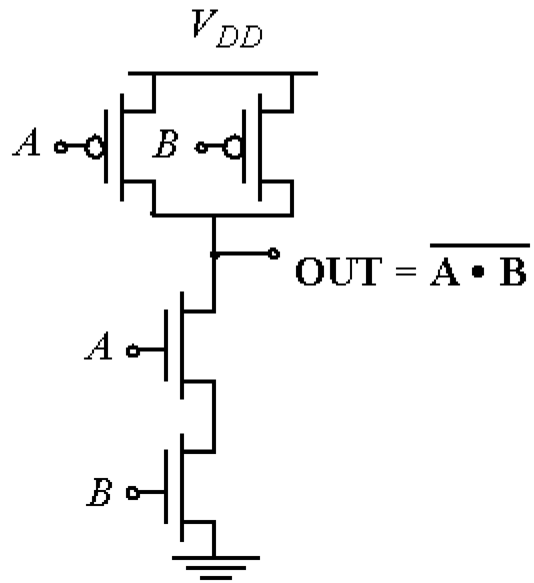
$Y = X$ if $\overline{A}$ OR $\overline{B} = \overline{AB}$

PMOS Transistors pass a "strong" 1 but a "weak" 0

Example Gate: NAND

A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

Truth Table of a 2 input NAND gate



PDN: $G = A\,B \Rightarrow$ Conduction to GND

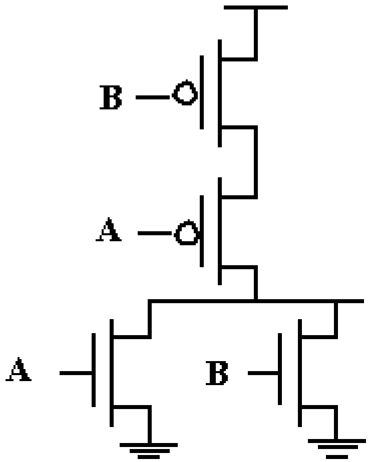
PUN: $F = \bar{A} + \bar{B} = \overline{AB} \Rightarrow$ Conduction to V_{DD}

$$\overline{G(In_1, In_2, In_3, \ldots)} \equiv F(\overline{In_1}, \overline{In_2}, \overline{In_3}, \ldots)$$

Example Gate: NOR

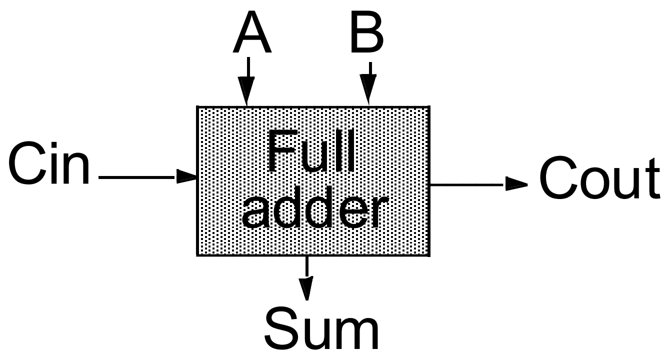
A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

Truth Table of a 2 input NOR gate



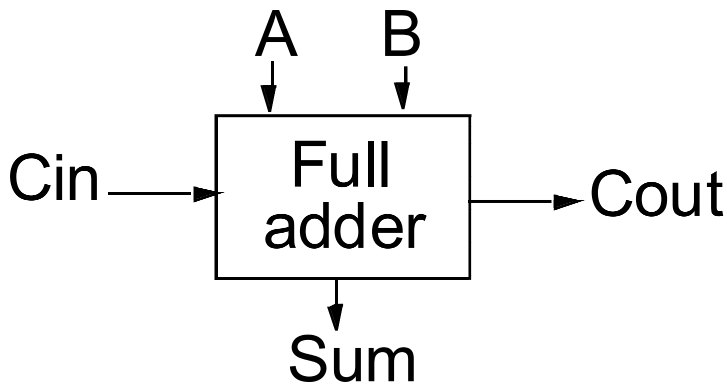
$$OUT = \overline{A + B}$$

Full-Adder



A	B	C_i	S	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The Binary Adder

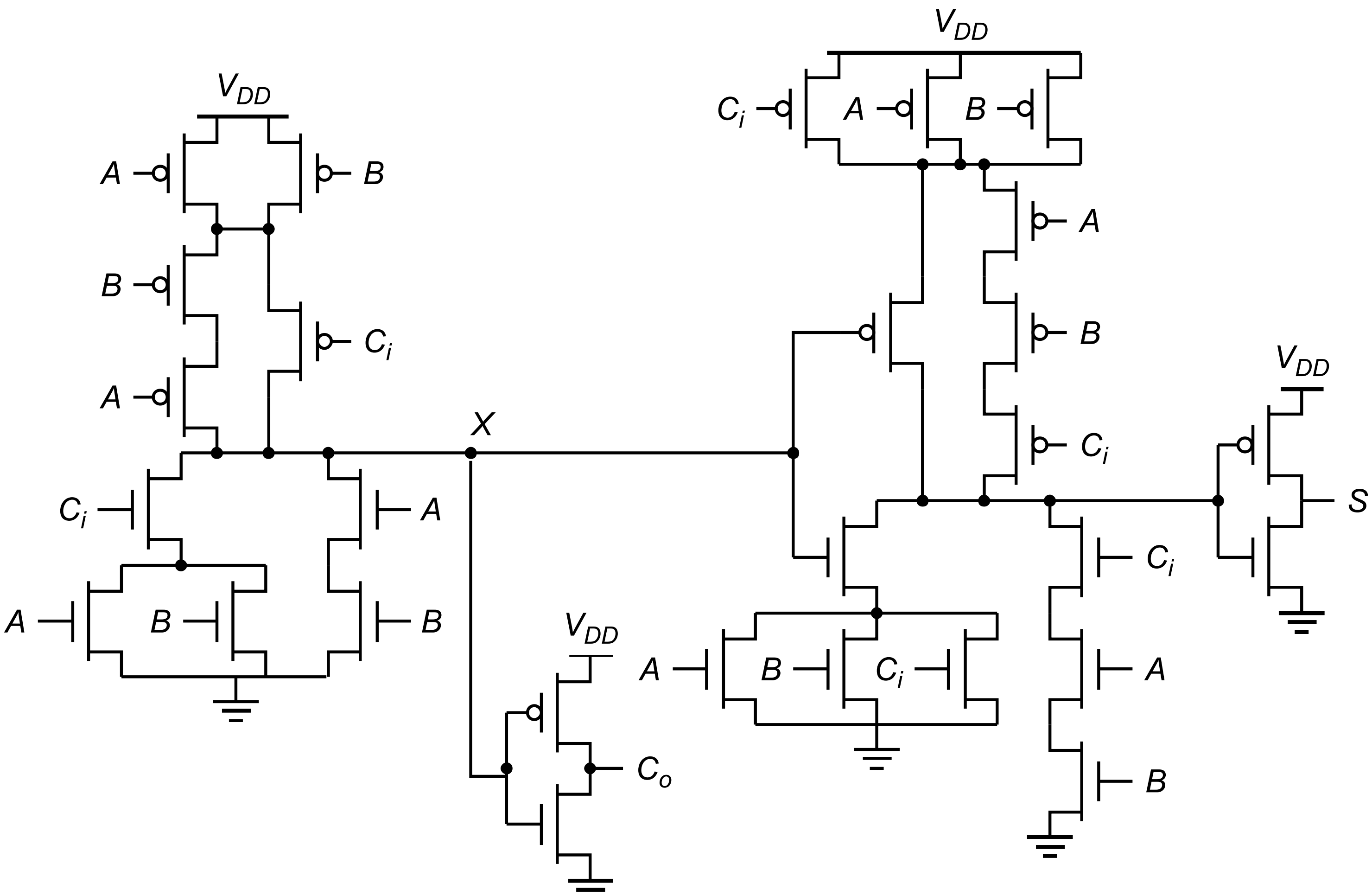


$$S = A \oplus B \oplus C_i$$

$$= A\bar{B}\bar{C}_i + \bar{A}B\bar{C}_i + \bar{A}\bar{B}C_i + ABC_i$$

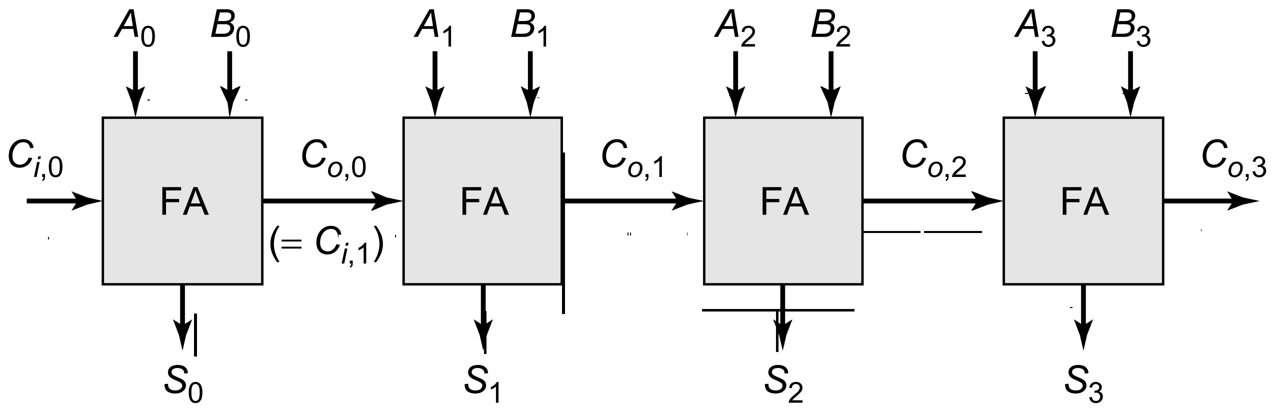
$$C_o = AB + BC_i + AC_i$$

Complimentary Static CMOS Full Adder

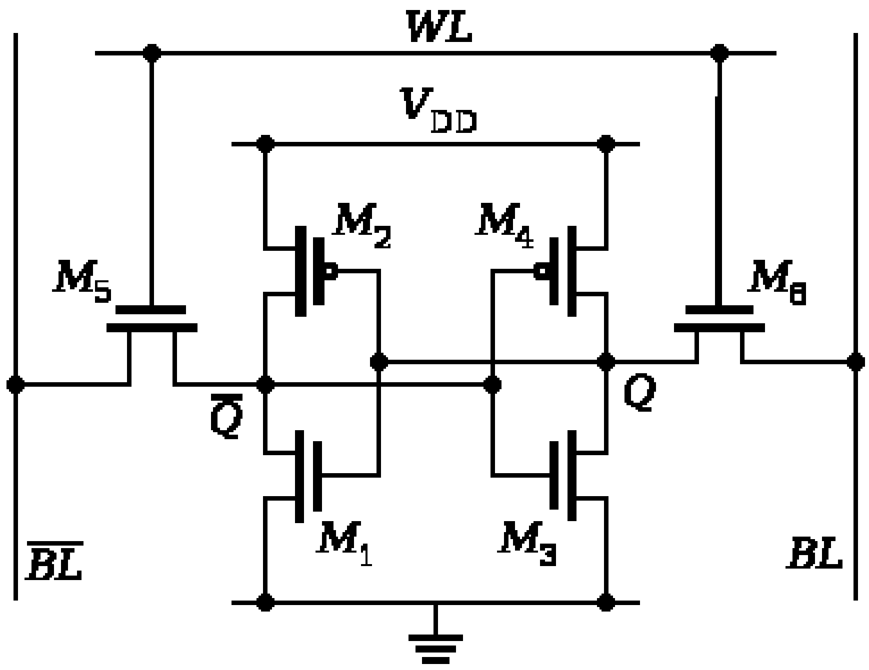


28 Transistors

The Ripple-Carry Adder



SRAM Memory cell

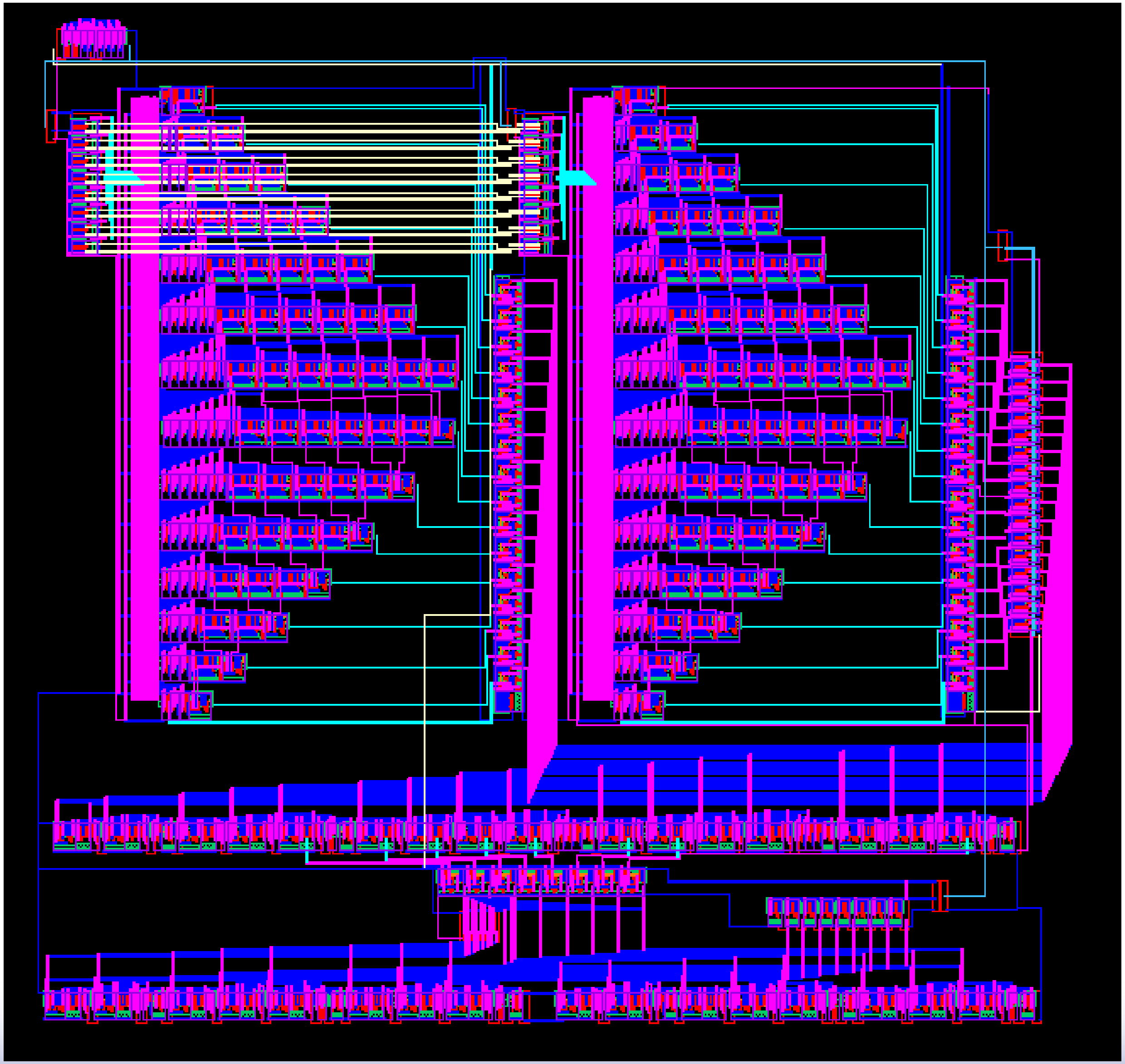


The add-up

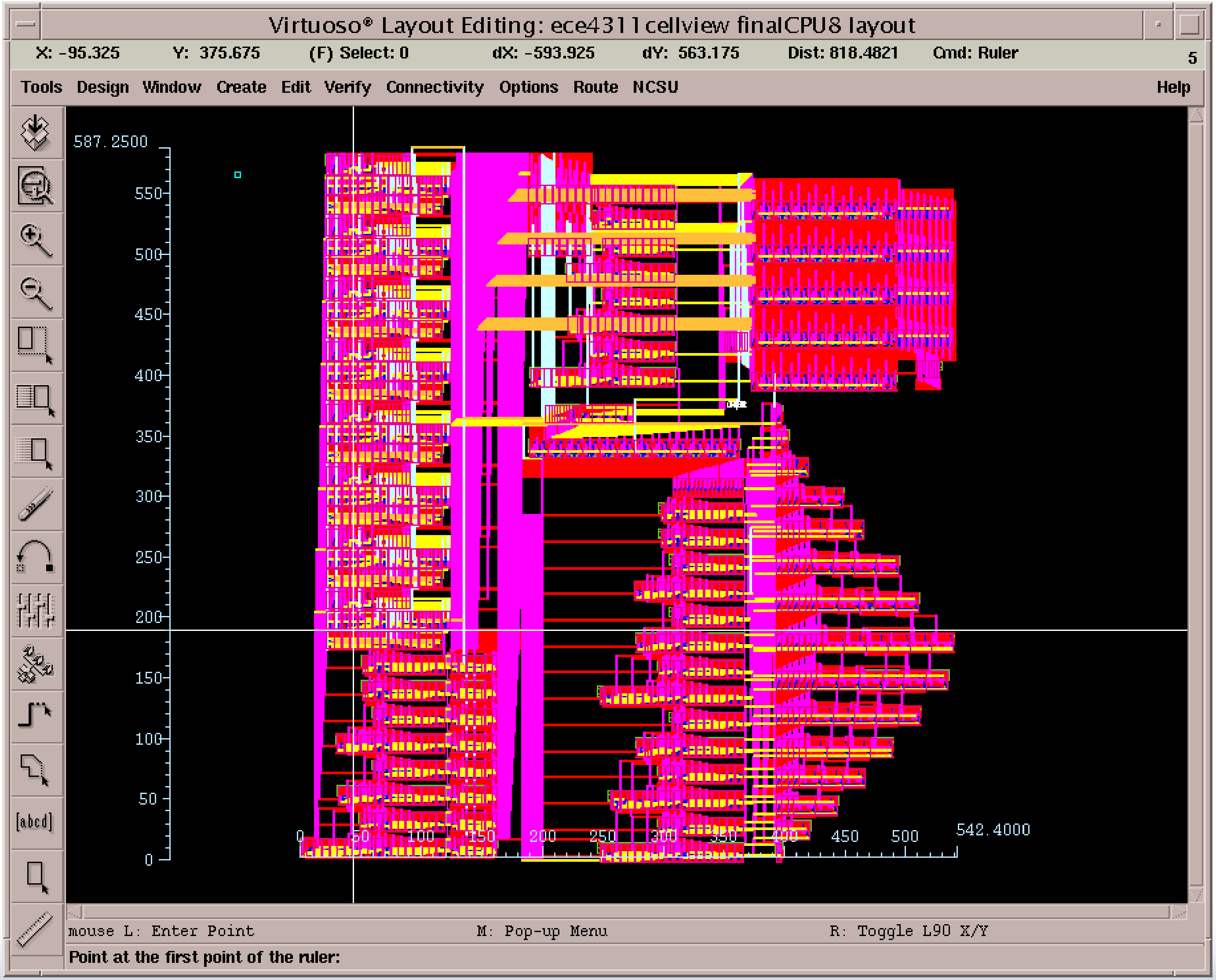
32-bit adder:	>3,000
32-bit comparator:	>3,000
32-bit multiplier:	>50,000
1k SRAM:	6,000

…

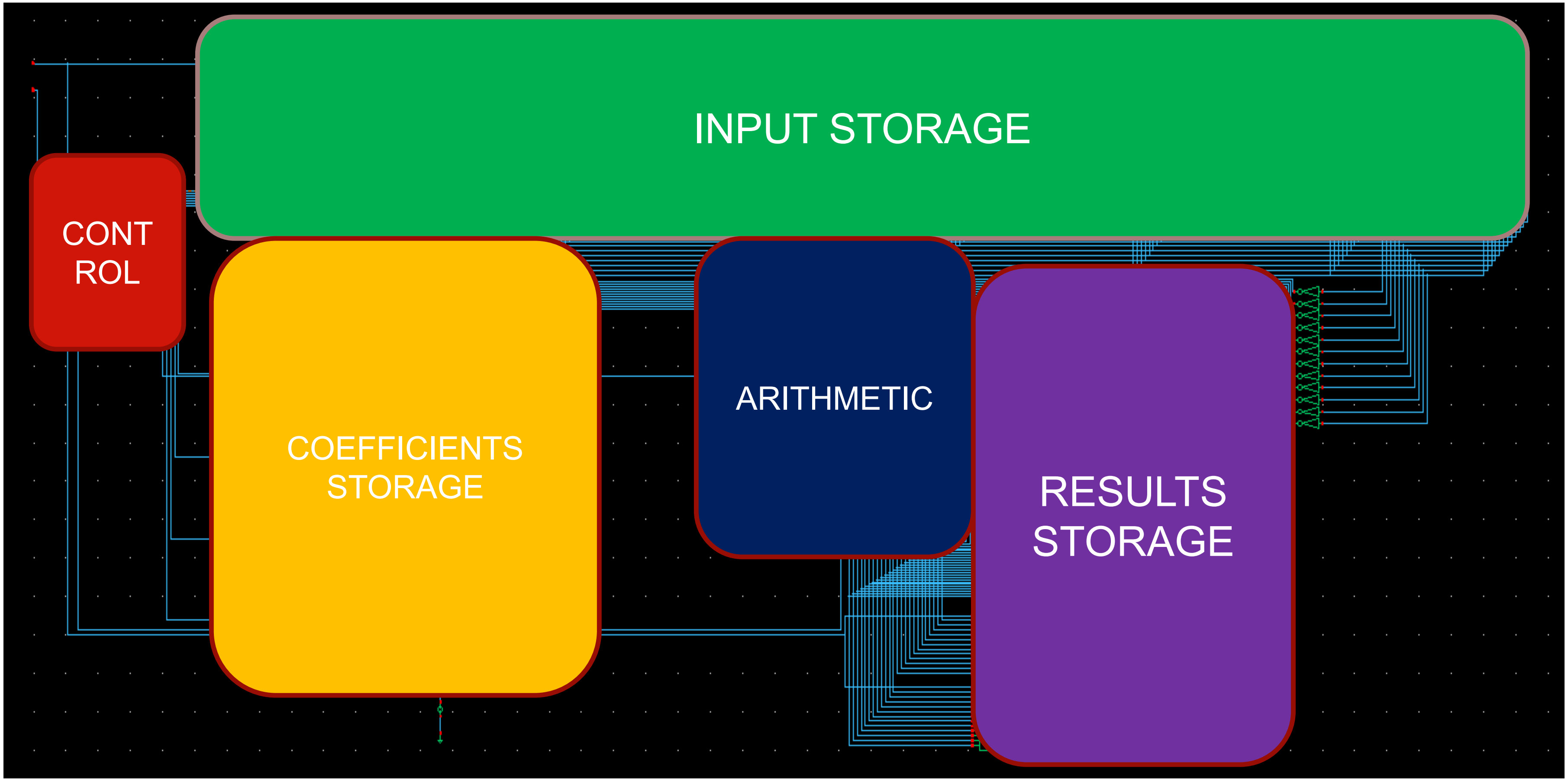
Example project: FFT Butterfly Unit Layout



8-bit CPU Layout



FIR Filter



Module 1 – Control Module

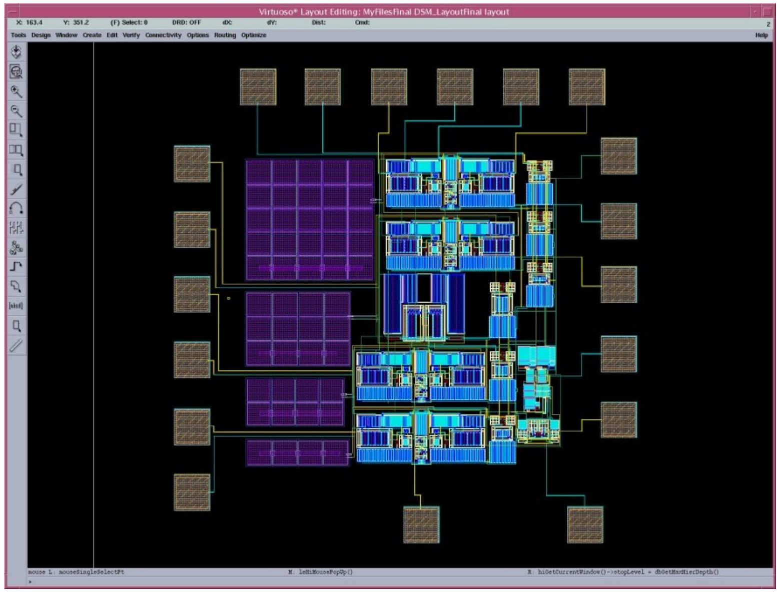
Module 2 – Input Module

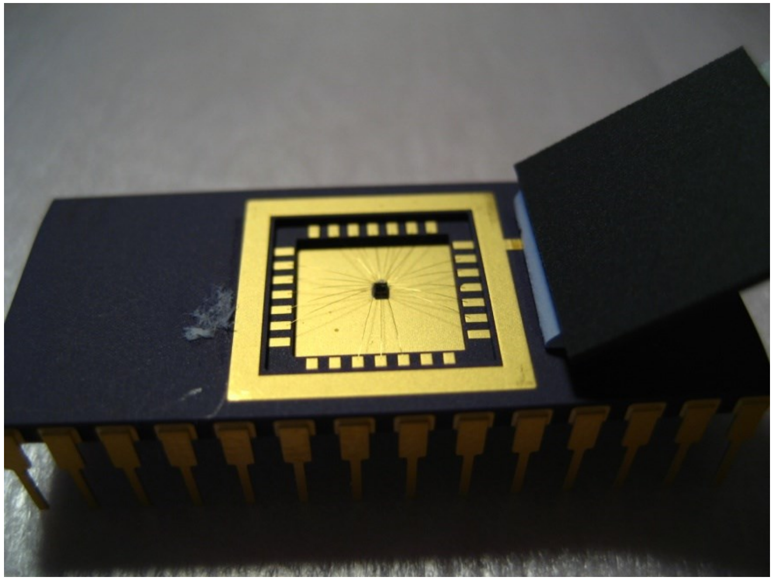
Module 3 – Coefficients Module

Module 4 – Arithmetic Module

Module 5 – Results Storage

A Delta-Sigma A/C Converter





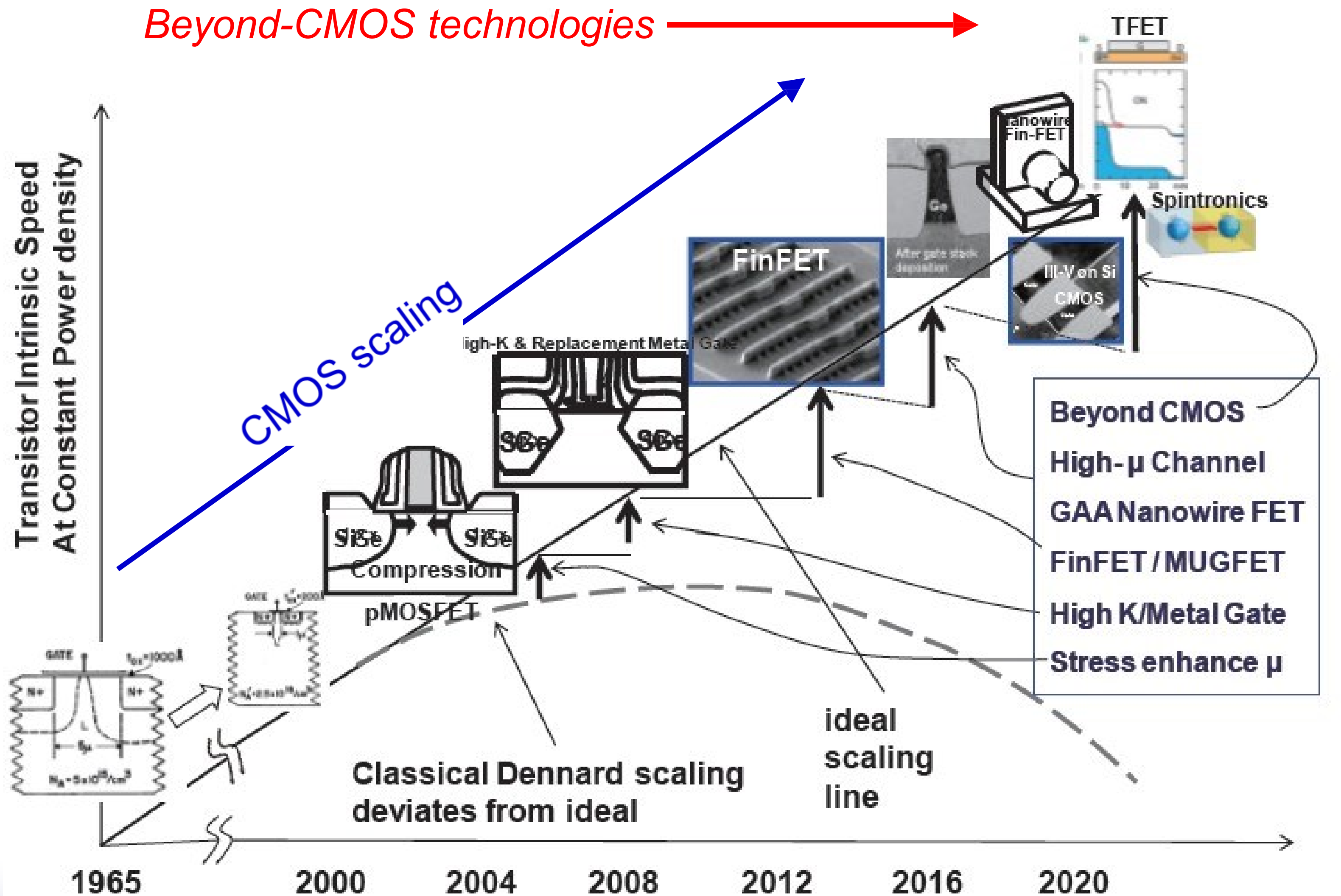
By: Matt Webb, Hairong Chang

Career in VLSI/IC

- Intel, AMD, Texas Ins.,,…
- National Semi., Cypress Semi,….
- Apple, Qualcomm, Broadcom, Samsung,…
- Micron, Seagate, WesternDigital…
- Cadence, Synopsys, MentorGraphics…
- Xilinx, Altera, ….

Picture from “Beyond-CMOS Technology Roadmap”, An Chen, Emerging Research Devices (ERD), ITRS

Technology Innovations Driven by Scaling



J. Y.C. Sun, VLSI Tech., T2 (2013)

Source: An Chen, ConFab 2015

Contact Information:

Office: MWAH 276

Hour: 10-11am, MTWF

Phone: 726-7095

Email: htang@d.umn.edu

Http: www.d.umn.edu/~htang