Sample-and-Hold Circuits

Chapter 11

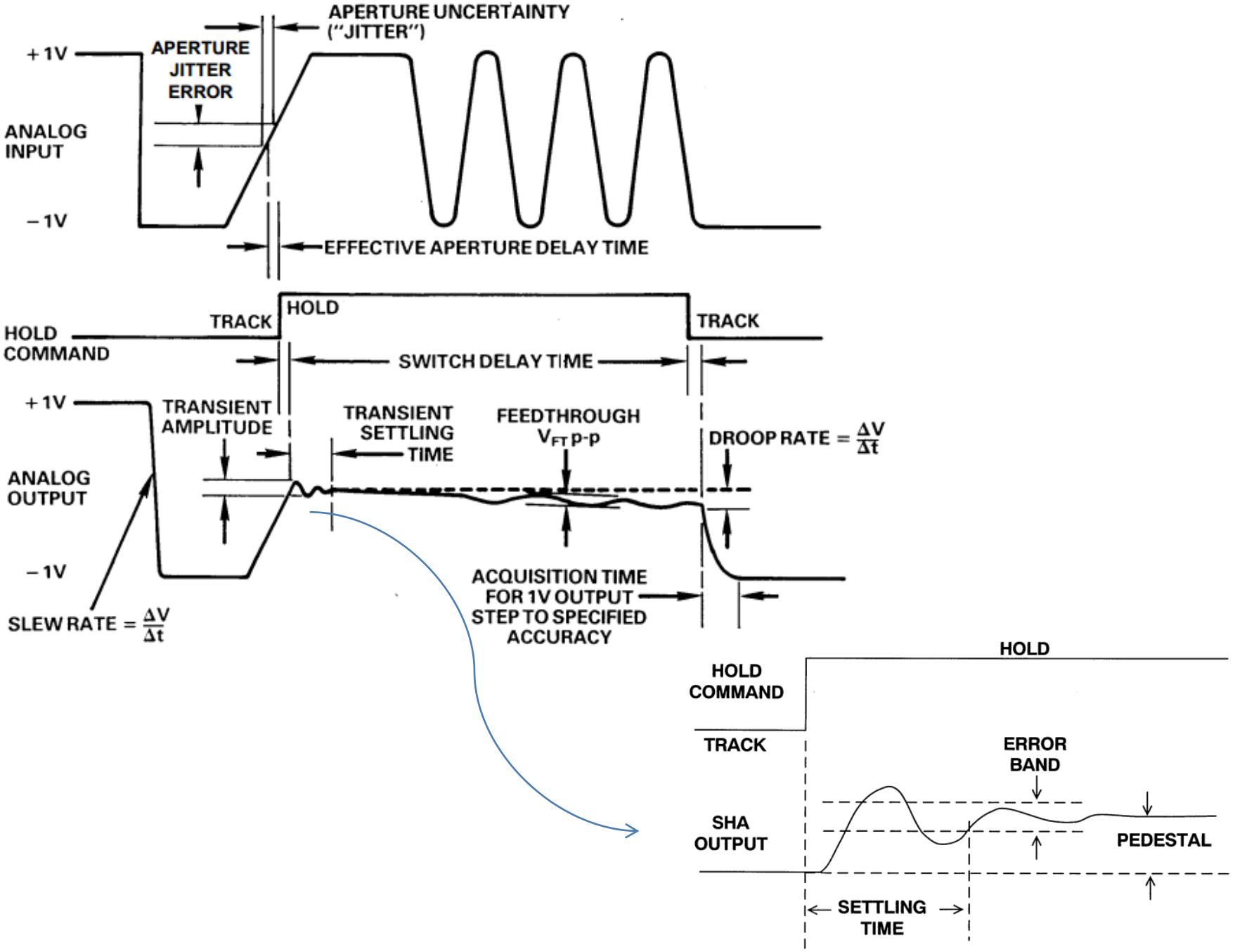
11.1 Introduction

Sample and hold circuits is used to sample an analog signal and to store its value for some length of time (for digital code conversion). It is heavily used in data converters.

Sample-and-hold are also referred to as track-and-hold circuits.

A few important performance parameters for sample-and-hold circuits:

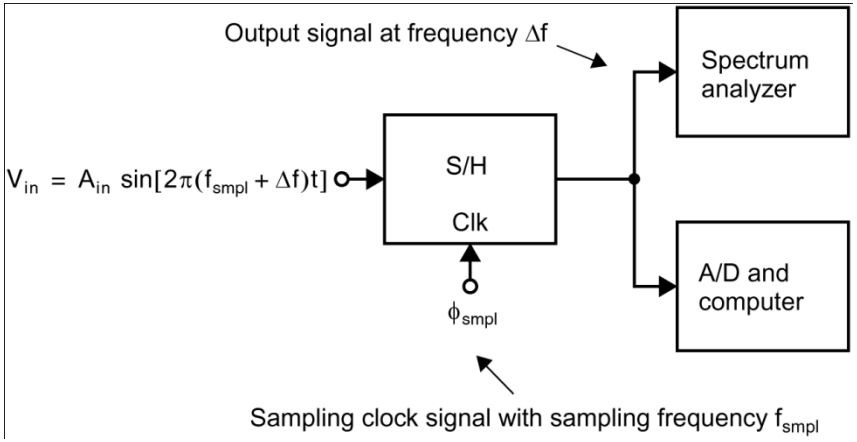
1. Sampling pedestal or hold step: occurs each time it goes from sample mode to hold mode and there is always a small error in the voltage being held that makes it different from the input voltage at the time of sampling. This error should be small and even more importantly be signal independent to avoid nonlinear distortion.
2. Another measure is called droop rate in hold mode, which characterizes a slow change in output voltage in hold mode.
3. Aperture jitter or uncertainty, which is a result of effective sampling time changing from cycle to cycle. When high-speed input signals are sampled, it causes the held voltage to be significantly different from the ideal held voltage.
4. The speed. When OpAmps are used, its 3dB bandwidth and slew rate should be maximized for high speed operation at the price of power consumption.
5. Other performance metrics, such as dynamic range, linearity, gain and offset error are important too.


APERTURE UNCERTAINTY
("JITTER")
+1V
APERTURE
JITTER
ERROR
ANALOG
INPUT
–1V
EFFECTIVE APERTURE DELAY TIME
HOLD
COMMAND
TRACK
HOLD
TRACK
SWITCH DELAY TIME
+1V
TRANSIENT
AMPLITUDE
TRANSIENT
SETTLING
TIME
FEEDTHROUGH
V_{FT} p-p
DROOP RATE = $\frac{\Delta V}{\Delta t}$
ANALOG
OUTPUT
–1V
SLEW RATE = $\frac{\Delta V}{\Delta t}$
ACQUISITION TIME
FOR 1V OUTPUT
STEP TO SPECIFIED
ACCURACY
HOLD
HOLD
COMMAND
TRACK
ERROR
BAND
SHA
OUTPUT
PEDESTAL
SETTLING
TIME

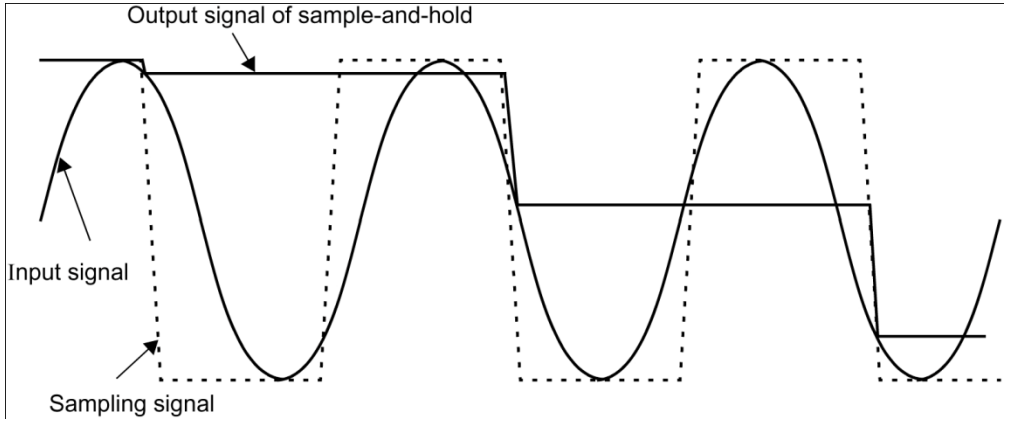
Testing of sample and hold

The beat test method is popular. In this test, the S&H circuit operates at its maximum clock frequency and apply a sinusoidal input signal that has a frequency slightly different than the clock frequency. The output is then demodulated to a low frequency equal to the difference between the frequency of the clock signal and that of the input signal, which is then analyzed using a spectrum analyzer or using FFT in computer.

This method is general to A/D converters too.



Chapter 11 Figure 01



Chapter 11 Figure 02

11.2 sample and hold basics

The simplest implementation of a S&H circuit is shown below.

The voltage V' would ideally stay constant in the hold mode by having a value equal to V_{in} at the instance of clock going low. But there are two error sources due to switch:

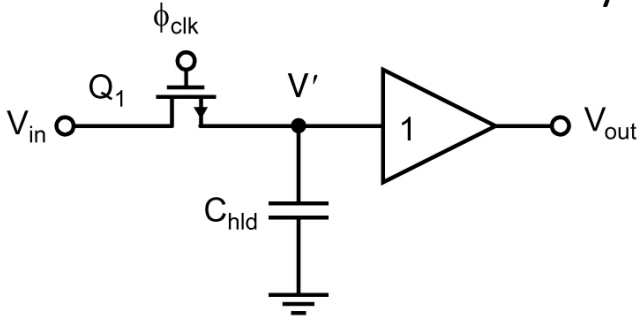
1. The channel charge go to both junctions to causes negative glitches. If source impedance of V_{in} is small, then the glitch is small and last a short duration.
2. The channel charge go to V' causes a negative voltage that is long lasting.

$$\Delta Q_{C_{hld}} = \frac{Q_{CH}}{2} = \frac{C_{ox}WLV_{eff\text{-}1}}{2} \qquad V_{eff\text{-}1} = V_{GS1} - V_{tn} = V_{DD} - V_{tn} - V_{in}$$

Here V_{in} is the input voltage at the moment Q1 turns off.

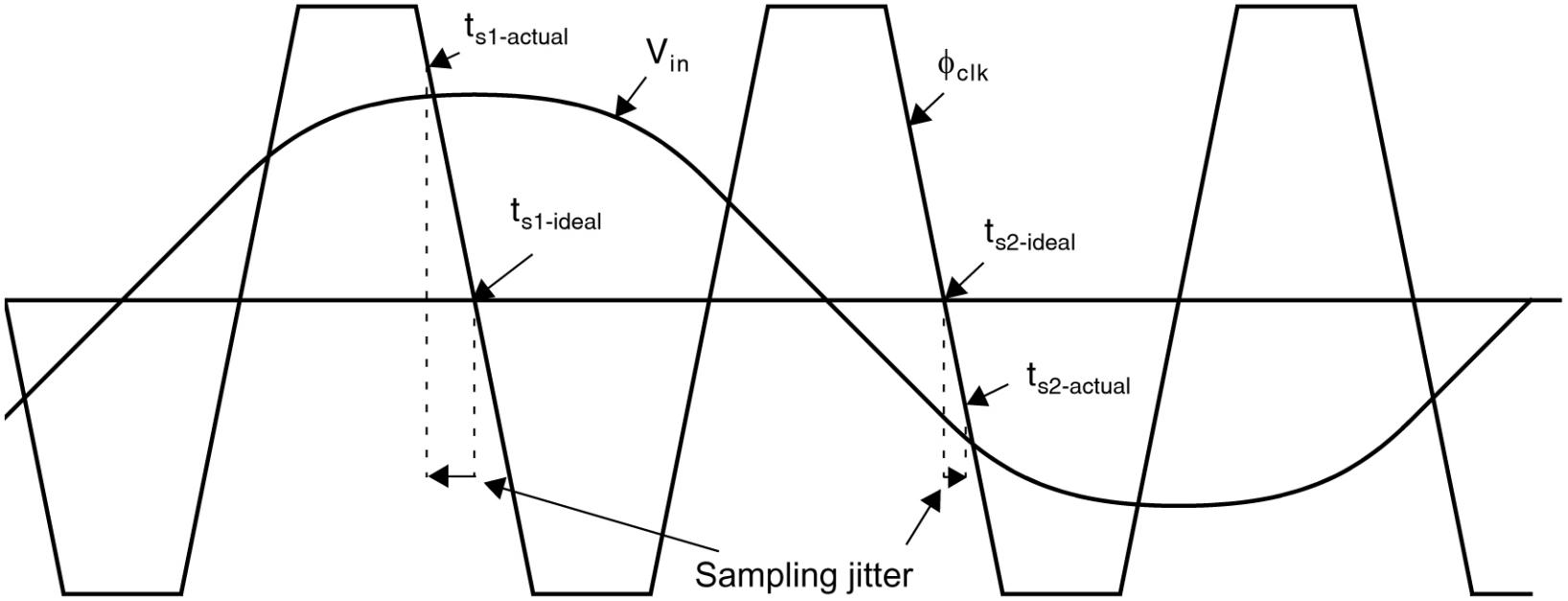
$$\Delta V' = \frac{\Delta Q_{C\text{-}hld}}{C_{hld}} = -\frac{C_{ox}WLV_{eff\text{-}1}}{2C_{hld}} = -\frac{C_{ox}WL(V_{DD} - V_{tn} - V_{in})}{2C_{hld}}$$

This error is linearly related to V_{in}, therefore causes a linear error (called gain error), but this error is also related to V_{tn}, which is nonlinearly related to V_{in} due to body effect and this nonlinearity causes harmonics.



Chapter 11 Figure 03

Aperture jitter due to clock waveforms



Chapter 11 Figure 06

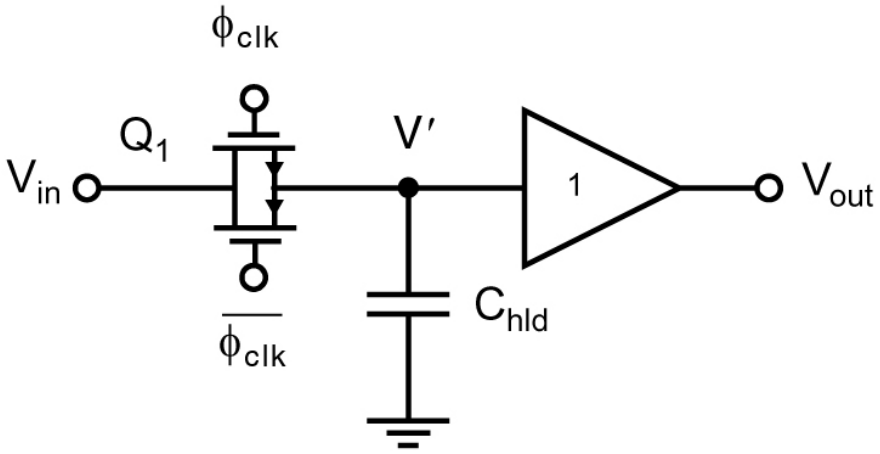
- When V_{in} is above 0V, the true sampling time is earlier than the ideal sampling time.
- When V_{in} is less than 0V, the true sampling time is late.

Methods to minimize the signal-dependent hold step

1. Replace nMOS by a CMOS transmission gate by a parallel of nMOS and pMOS controlled by the clock and inverse of the clock. The idea behind this is that if the size of the pMOS is taken the same as the nMOS, then the charge injection due to each transistor will cancel when the transmission gate turns off.

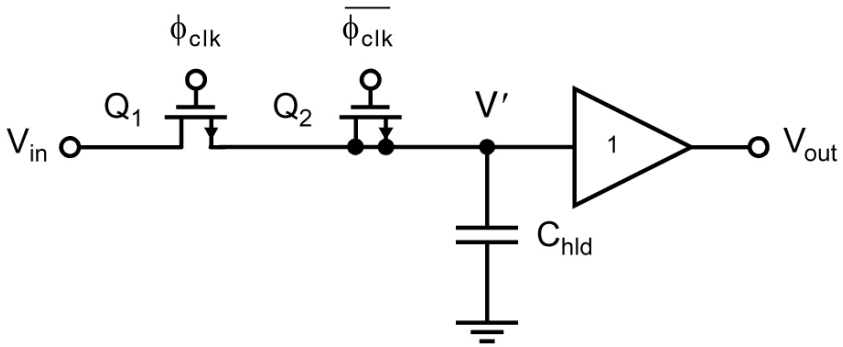
Two drawbacks:

- transistor turn-off times are signal dependent and this signal dependence causes the n-channel transistor to turn off at different times than the p-channel transistor.
- p and n have different amount of channel charges, e.g., when V_{in} is closer to V_{DD} , the charge from the p-channel transistor is greater than that from the n-channel transistor



Chapter 11 Figure 04

2. Using a dummy switch that is ideally half of the size of Q1. As Q2 goes from low to high, so the charge of Q2 ideally cancels that of Q1 from high-to-low.
   - When clock waveforms are fast, this technique usually can minimize the hold pedestal to less than about one-fifth the value it would have without it.
   - The clock of Q_2 changes slightly after that of Q_1. This guarantees that the cancelling charge of Q_2 can't escape through Q_1.

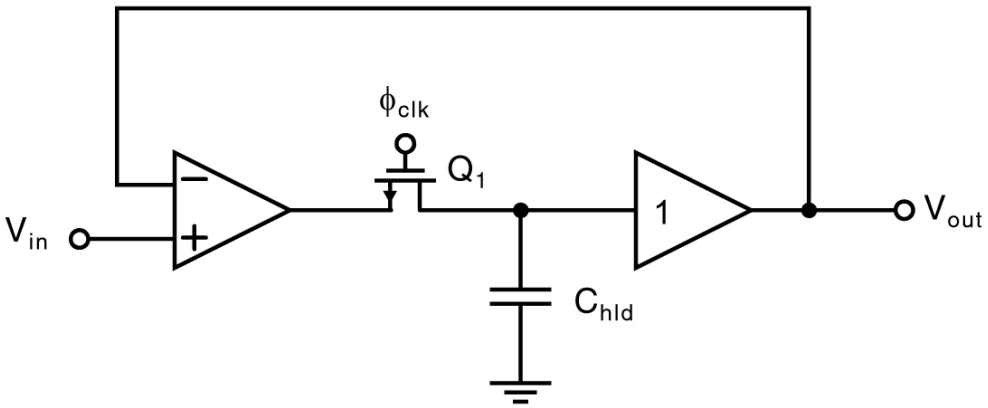


Chapter 11 Figure 05

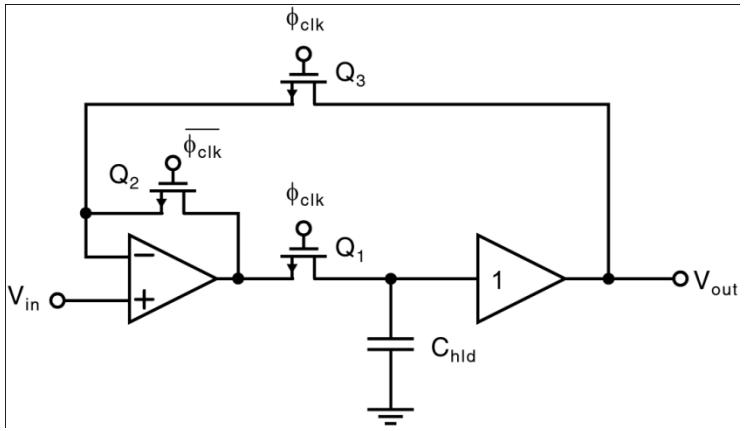
A more elaborate sample-and-hold circuit is to include an OpAmp in the feedback loop. By including an OpAmp in the loop, the input impedance of the sample and hold is greatly increased. Another advantage is that the offset voltage of the unity-gain buffer is referred to the input by the gain of the OpAmp. So a simple source follower can be used.

- The speed of operation can be seriously degraded due to the necessity of guaranteeing that the loop is stable when it is closed.
- When in hold mode, the OPAMP is open loop, resulting in its output almost certainly saturating at one of the power supply voltages.

When the S/H goes back into track mode, it will take some time for the OPAMP output to slew back to its correct closed-loop value. This slewing time can be greatly minimized by adding two additional transistors

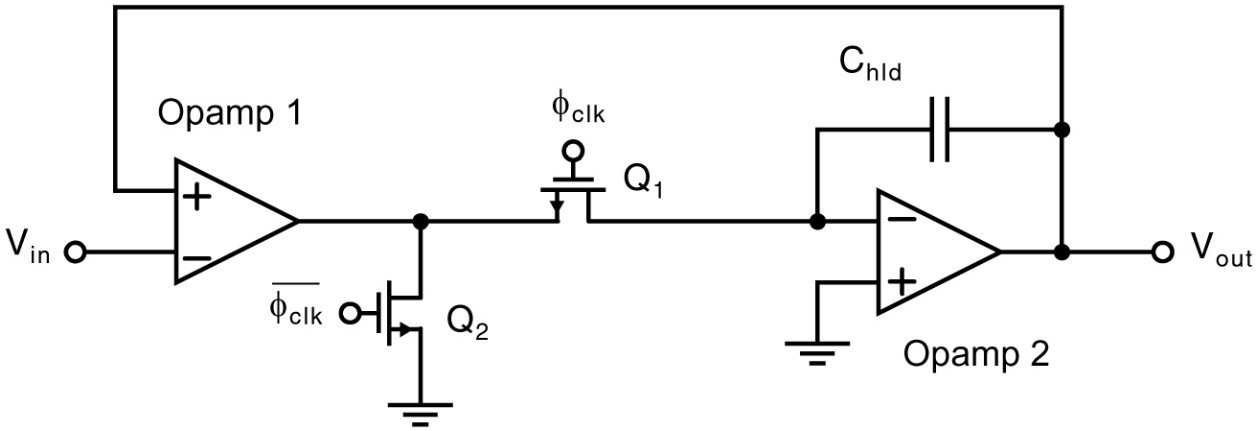


Chapter 11 Figure 07

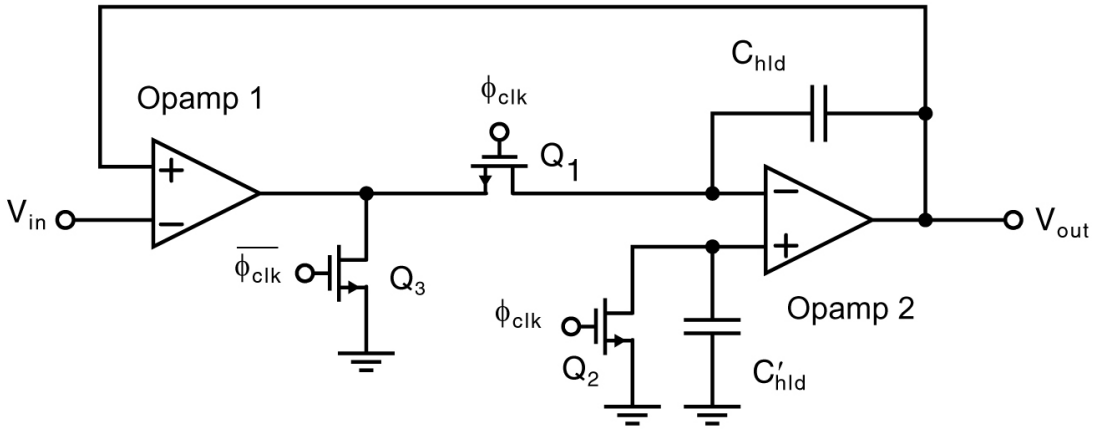


Chapter 11 Figure 08

An improved sample and hold circuit by using two OpAmps. Here the hold capacitor is placed in the feedback path of a second OpAmp. The advantage is that now both sides of Q1 is almost signal independent if OpAmp2 has a large gain. So, when Q1 turns off, there is still charge going to capacitor, but the V_{out} will have only a fixed DC error voltage.



Chapter 11 Figure 09



Chapter 11 Figure 10

Match the charge injection error to both capacitors, which is rejected by the differential amplifier.