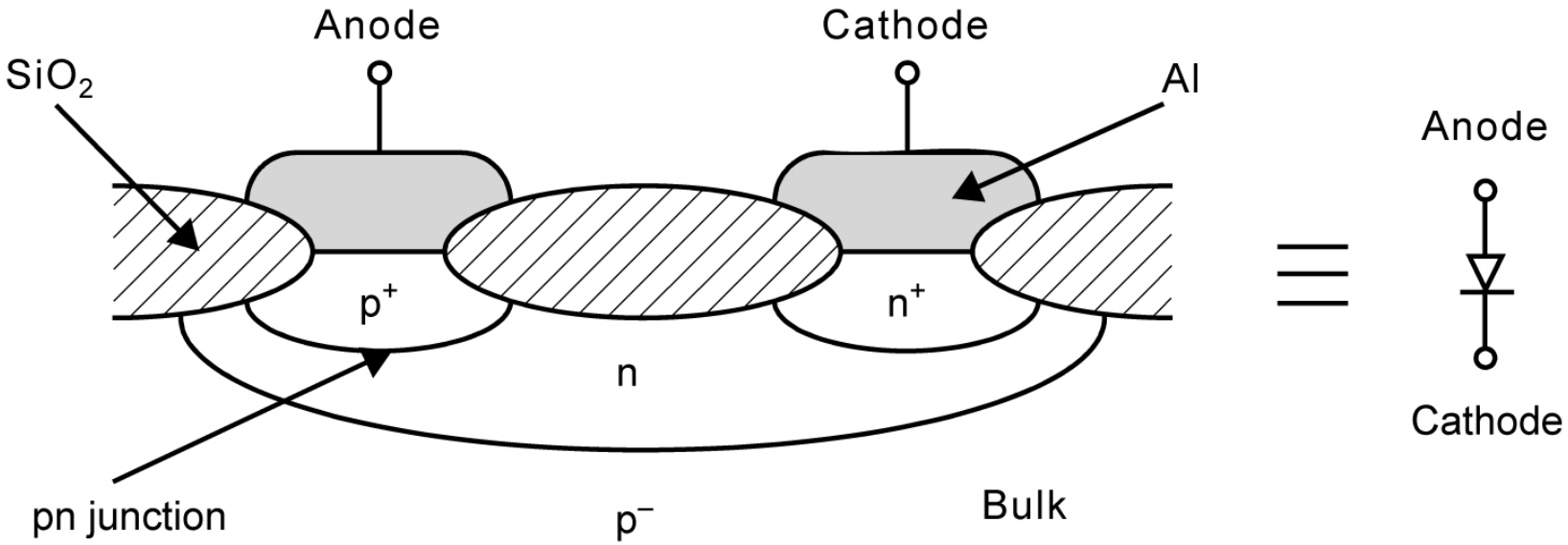
Today's topic:

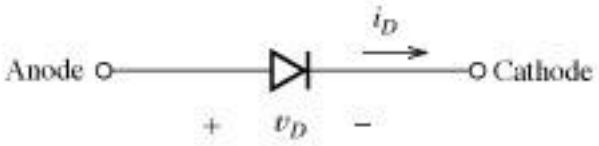
Integrated devices and modeling (with focus on MOS transistor) (Chapter 1)

A. Diode
B. BJT
C. MOSFET
D. Resistor
E. Capacitor
F. SPICE modeling

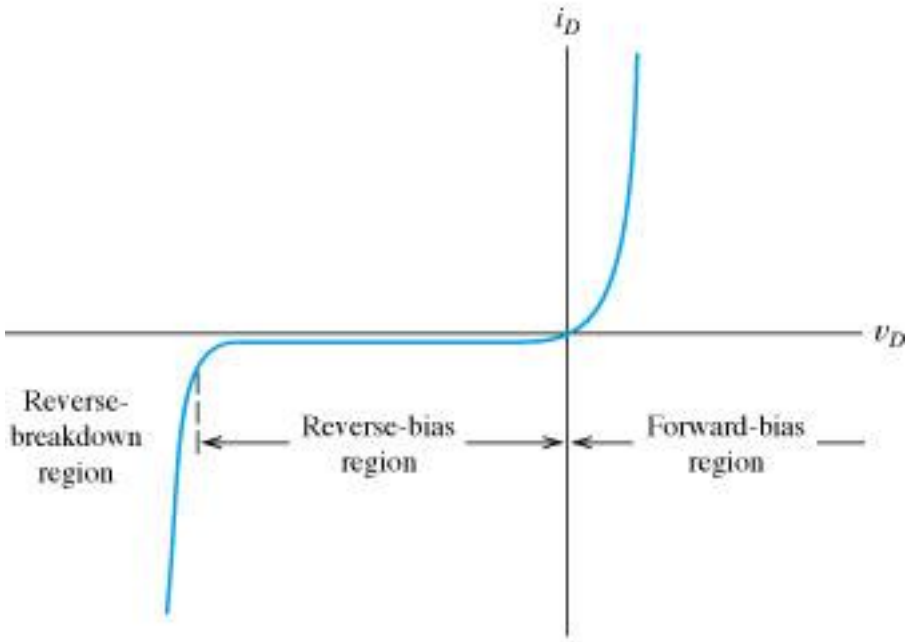
Cross section view of a Diode



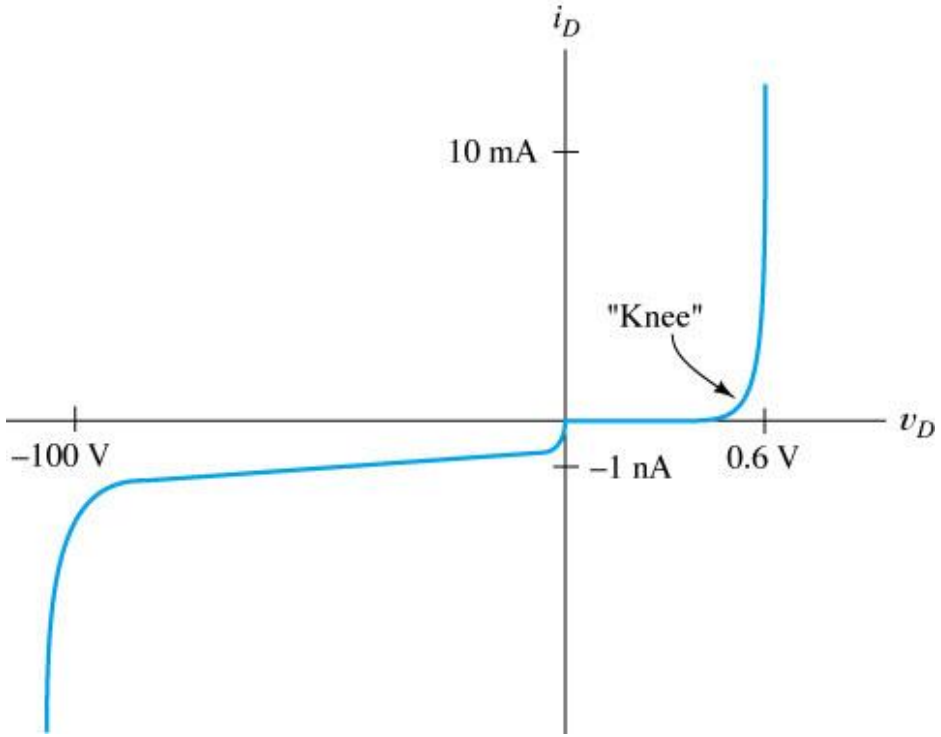
Voltage-current relation of a Diode



(a) Circuit symbol



(b) Volt-ampere characteristic



Linear small-signal equivalent circuit

- Many electronic circuits use DC supply voltages to bias a nonlinear device at an operating point and a small AC signal is injected into the circuit.
- In this case, analysis of the circuit can be split to two parts.
- First, DC analysis to find the operating point. In this part, nonlinear characteristics of the device must be considered.
- Second, AC (or small-signal) analysis is performed. In this part, the device characteristics are approximately linear if sufficiently small regions of operation is considered, a small linear small-signal equivalent circuit for the nonlinear device can be used for analysis.
- Small-signal linear equivalent circuit is a very important analysis approach that applies widely to electronic circuits.

Small-signal equivalent circuit of Diodes

• In the case of diodes, DC supply voltage bias the diodes at the quiescent point, or called Q-point.

• At the Q-point, a small AC signal injected into the circuit swings the instantaneous point of operation slightly above and below the Q-point. For sufficiently small AC signal, the characteristics is straight.

We can define then

$$\Delta i_D = (di_D / dv_D)_Q \Delta v_D$$

$$r_d = [(di_D / dv_D)_Q]^{-1}$$

$$\Delta i_D \approx \Delta v_D / r_d$$

•Therefore, one can find the equivalent resistance of the diode from the small AC signal.

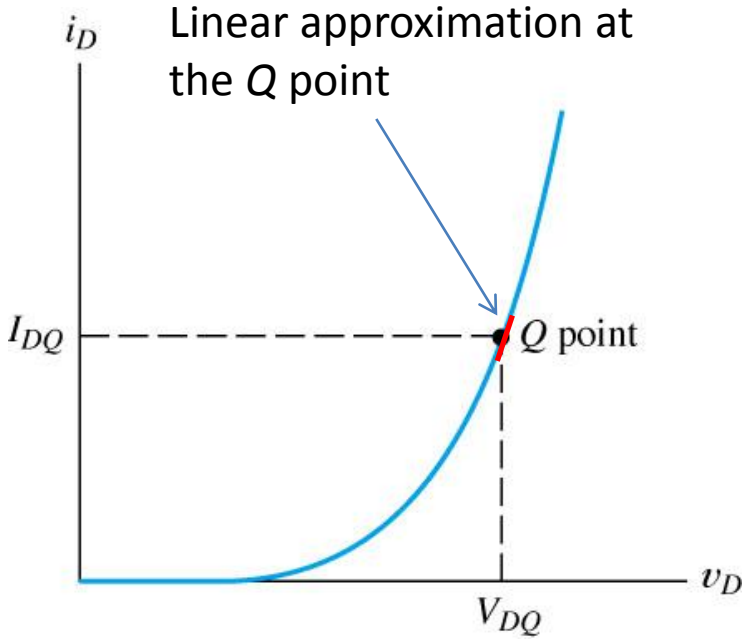


Figure 3.31 Diode characteristic illustrating the Q-point.

Depletion capacitance of diode

Under reverse bias, the depletion region get wider with increasing voltage.

The charge in the depletion region is similar to the charge stored on a parallel-plate capacitor. However, additional charge increment in the depletion region is separated by a larger distance.

Thus the reverse bias junction behaves like a capacitor, but depletion region capacitance is not constant (or nonlinear).

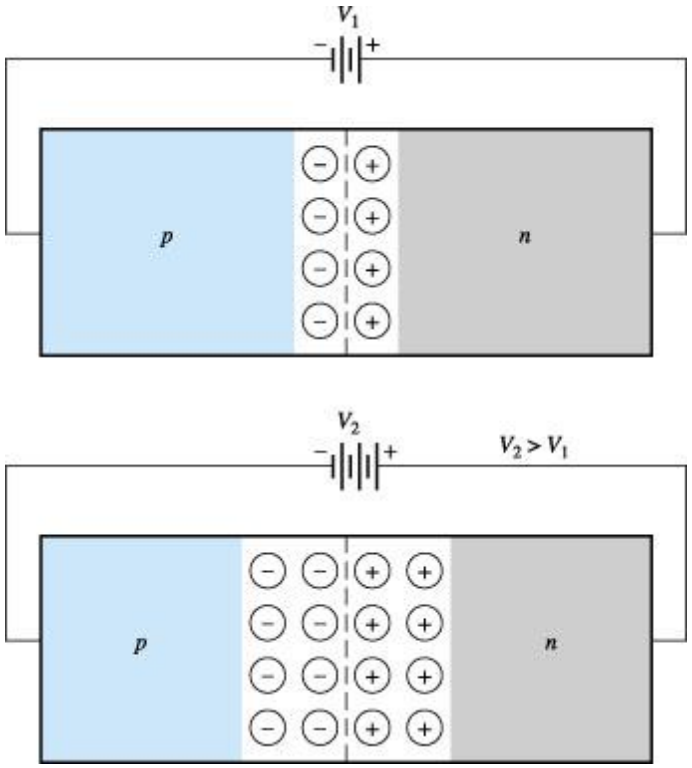


Figure 3.47 As the reverse bias voltage becomes greater, the charge stored in the depletion region increases.

Depletion capacitance of diode II

The depletion region capacitance is defined as

$$C_j = \frac{dQ}{dv_D}$$

$$C_j = \frac{C_{j0}}{[1 - V_{DQ} / \phi_{0)}]^m}$$

C_{j0} depletion capacitance for zero bias voltage

V_{DQ} operationg point voltage

ϕ_0 built-in barrier potential $\Phi_0 = V_T \ln\left(\frac{N_A N_D}{n_i^2}\right)$

m grading coefficient

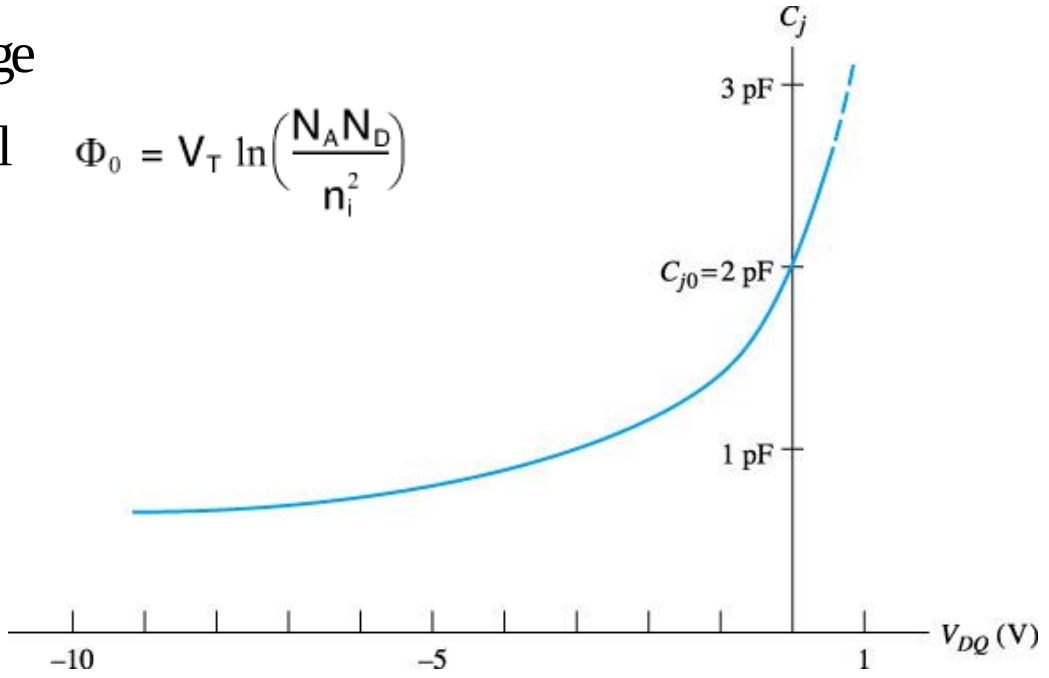


Figure 3.48 Depletion capacitance versus bias voltage for the 1N4148 diode.

Diffusion capacitance of diode

Another basic charge-storage mechanism occurs when the PN junction is forward biased.

For p^+n junction (p type is more heavily doped) shown below, the current crossing the junction is mainly due to holes from the p-side to n-side. The charge associated with the holes that have crossed the junction is stored charge (represented in shaded area below). As current is increased, more holes cross the junction and stored charge increases.

This effect of charge storage is represented as diffusion capacitance.

$$C_{dif} = \frac{\tau_T I_{DQ}}{V_T}, \tau_T \text{ average lifetime of minority carriers,}$$
$$I_{DQ} \text{ operating point diode current, } V_T \text{ thermal voltage}$$

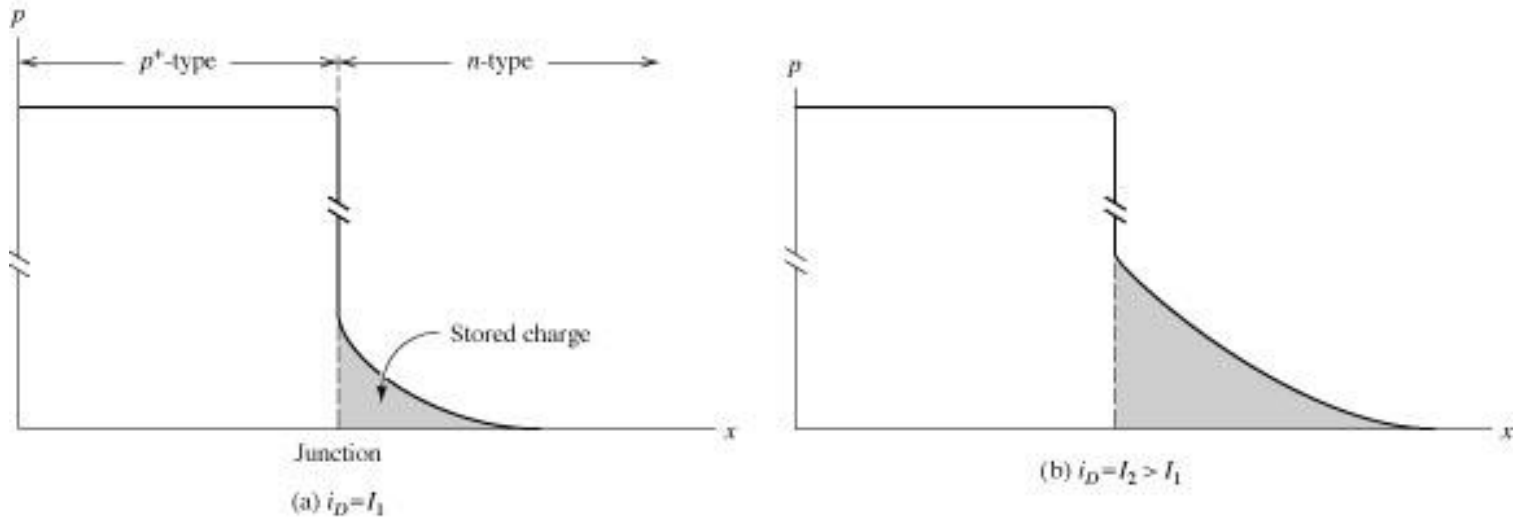


Figure 3.49 Hole concentration versus distance for two values of forward current.

Complete small-signal model of diode

- Complete small-signal model can be derived.

  R_s ohmic resistance of bulk material on both sides of the PN junction

  r_d small-signal resistance of the diode

  C_j depletion capacitance

  C_{dif} diffusion capacitance

- Under reverse bias, C_{dif} is 0 and r_d is an open circuit.

- This small-signal equivalent circuit is valid for PN junction diode over a wide range of frequencies provided small-signal conditions apply.

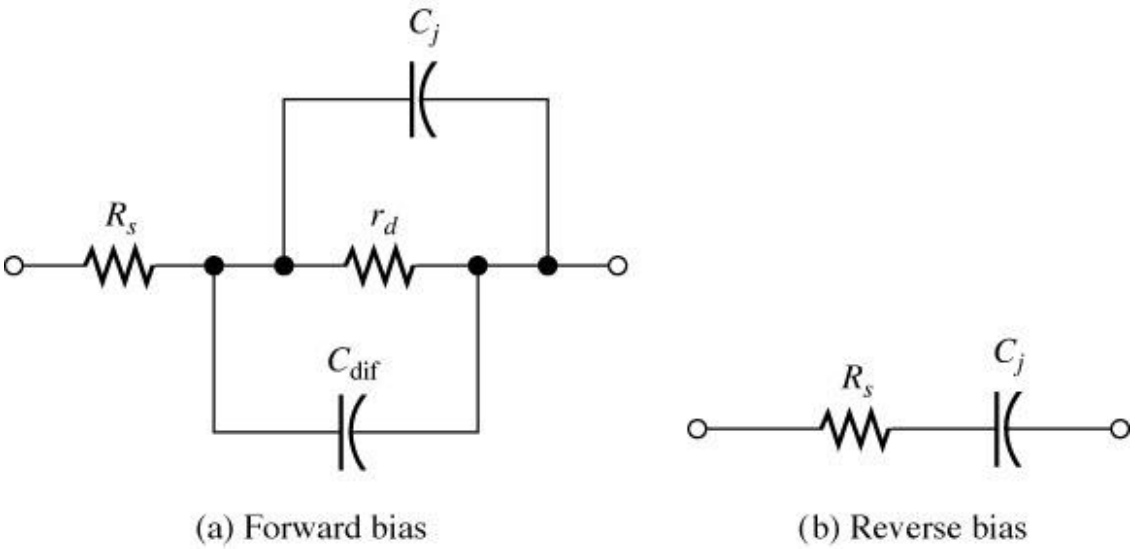
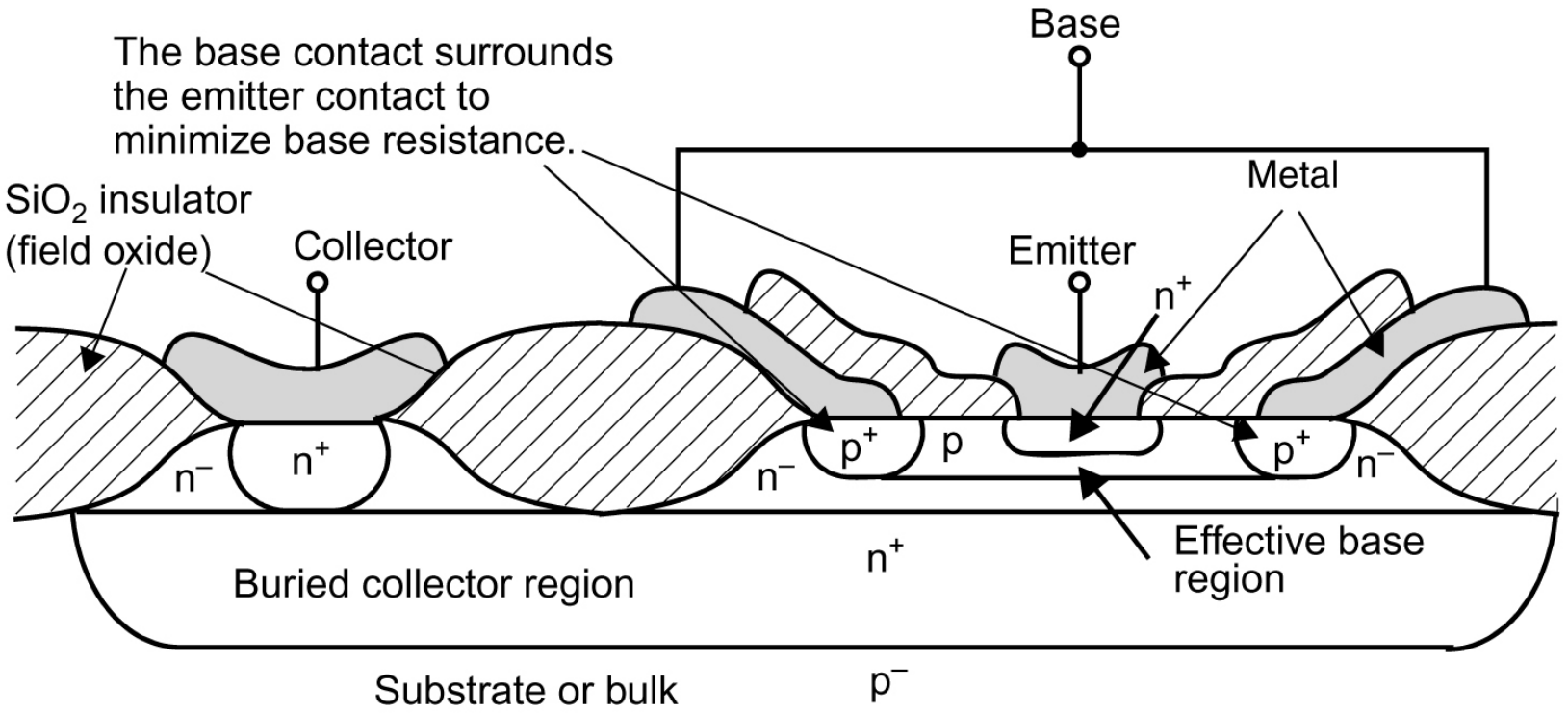


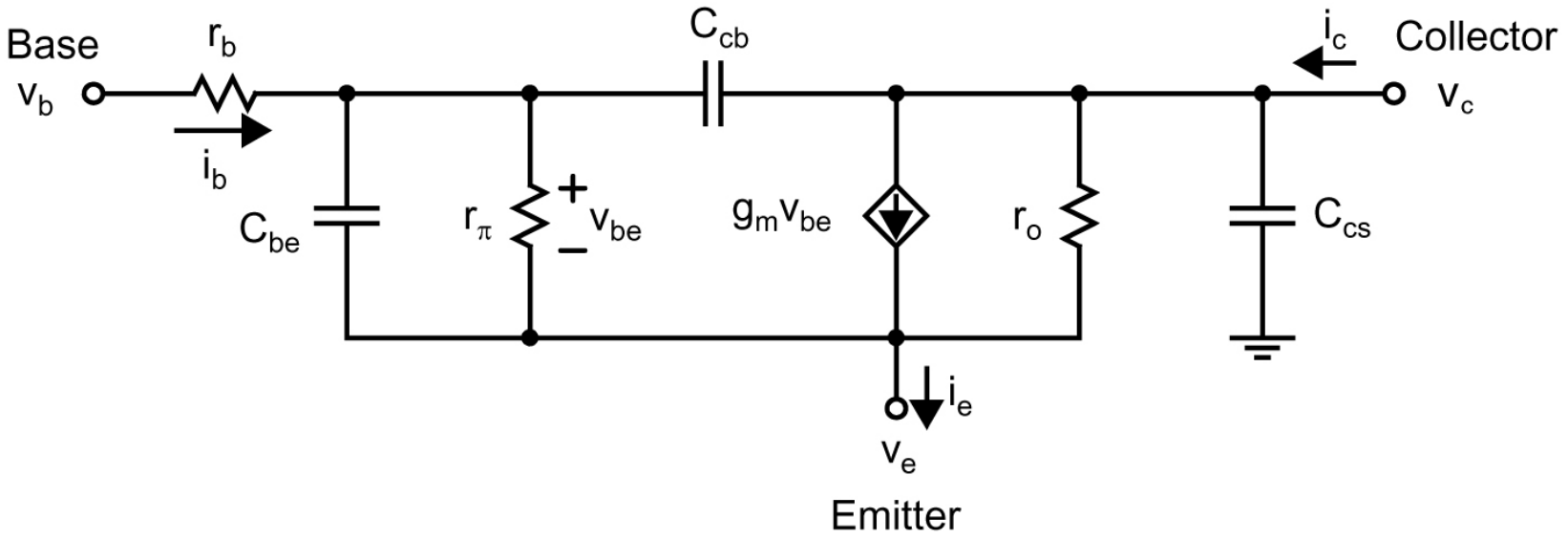
Figure 3.50 Small-signal linear circuits for the *pn*-junction diode.

Cross section view of a BJT transistor



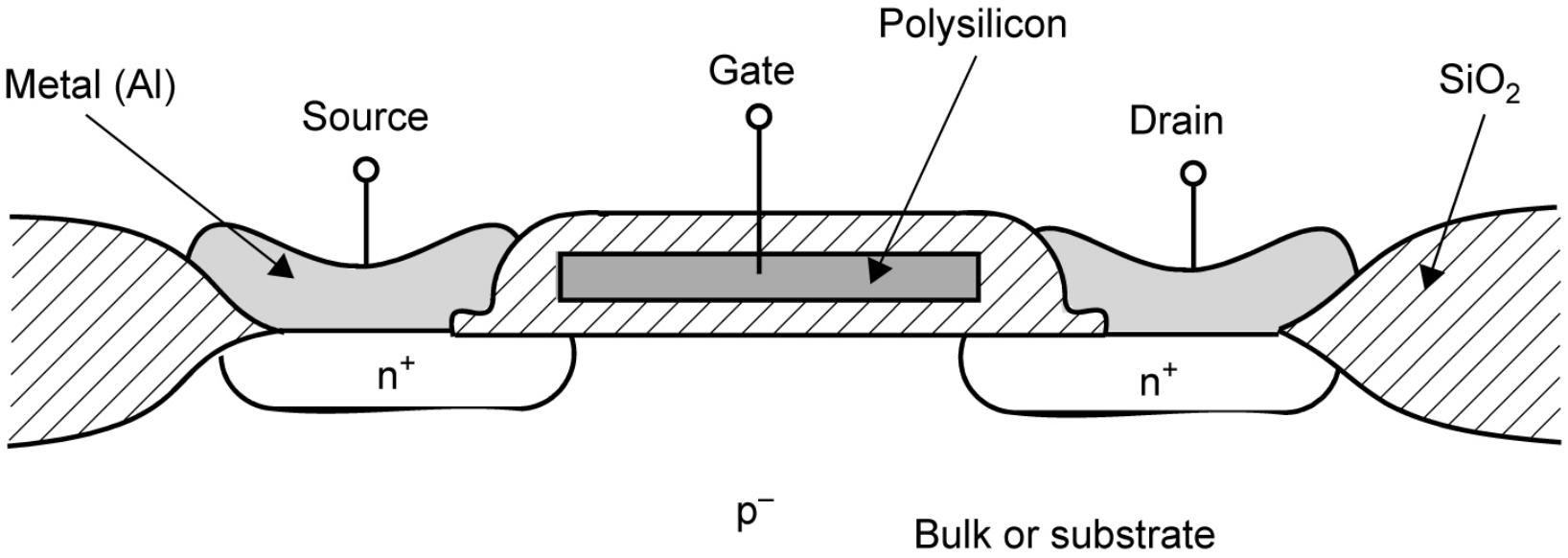
Chapter 8 Figure 01

Small-signal model of a BJT transistor

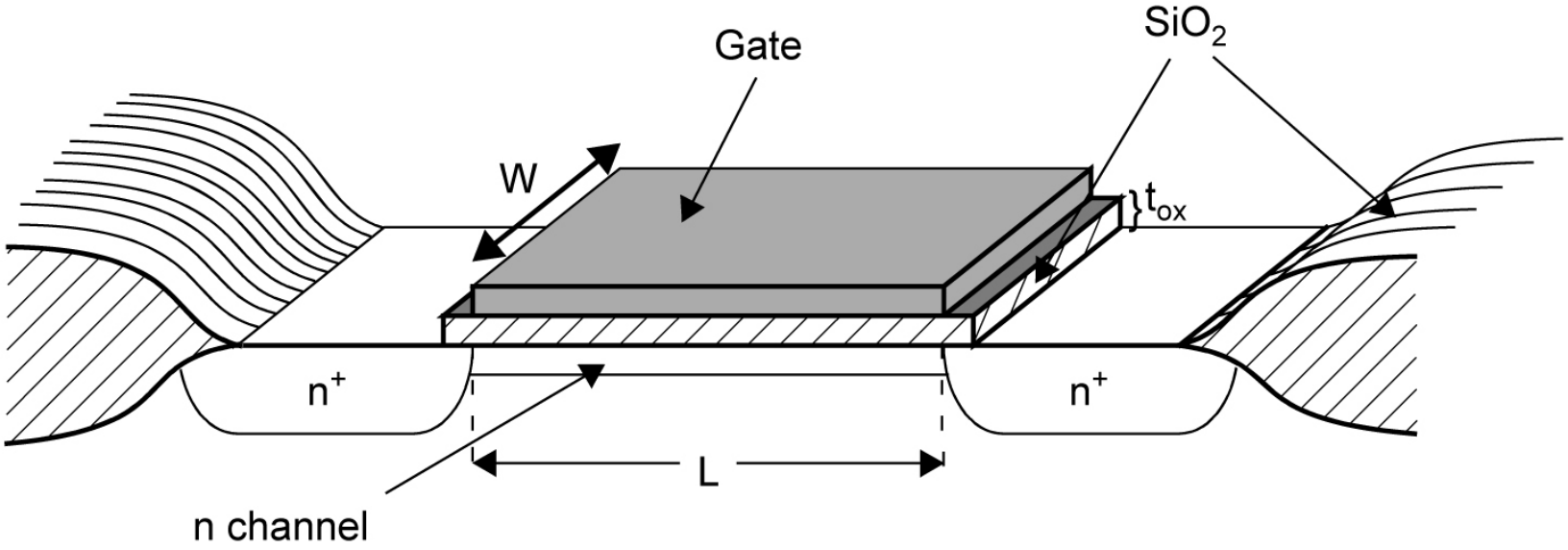


Chapter 8 Figure 08

Cross section view of a MOS transistor

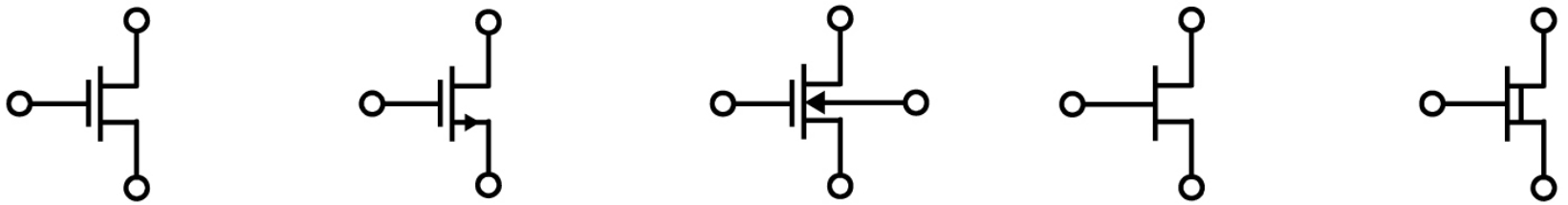


The important dimension of a transistor

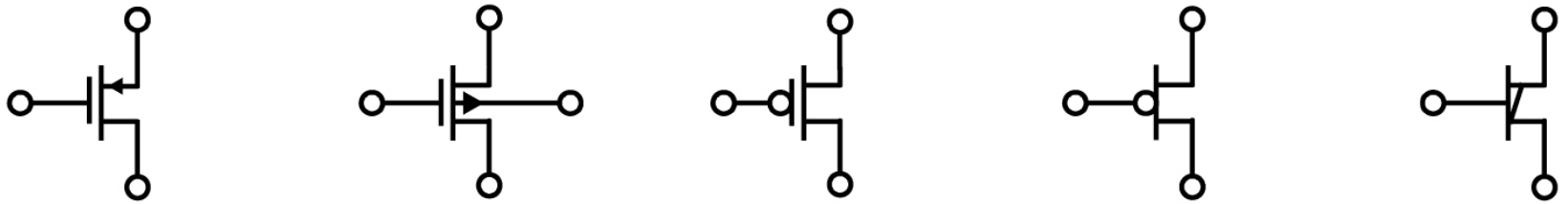


Chapter 1 Figure 10

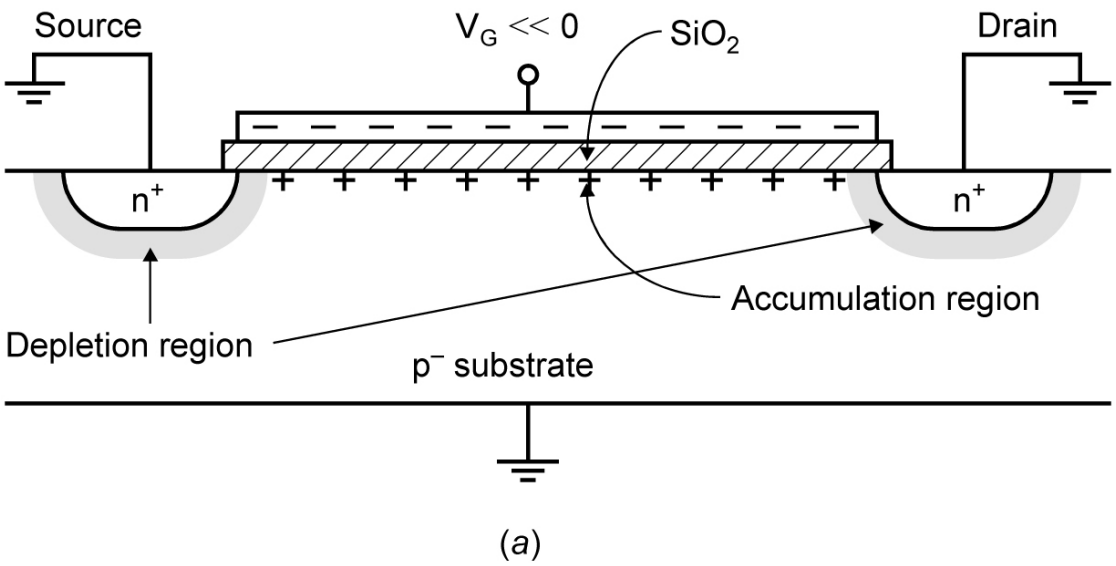
MOS transistor symbols (NMOS)



MOS transistor symbols (PMOS)

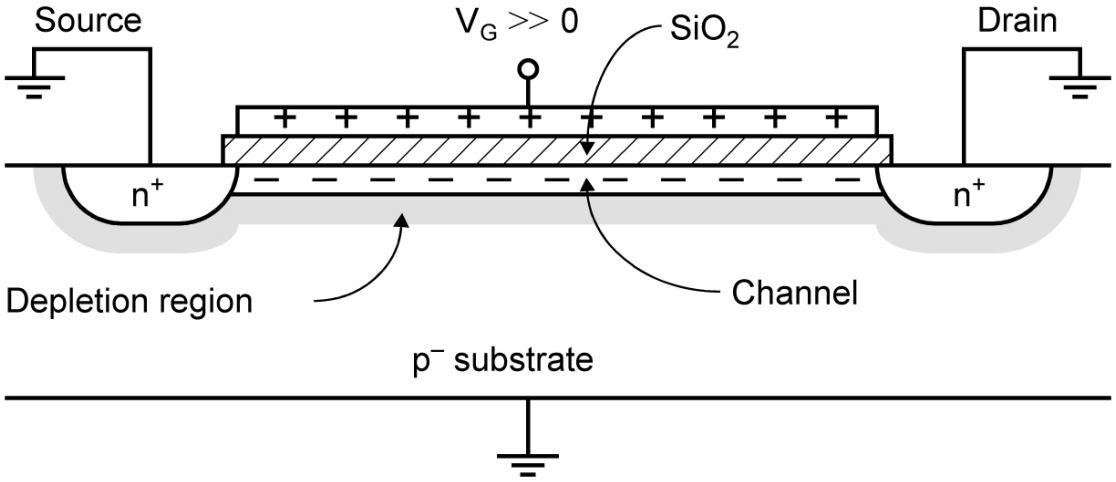


Transistor operation I



(*a*)

Resulting in an accumulated channel but no current flow

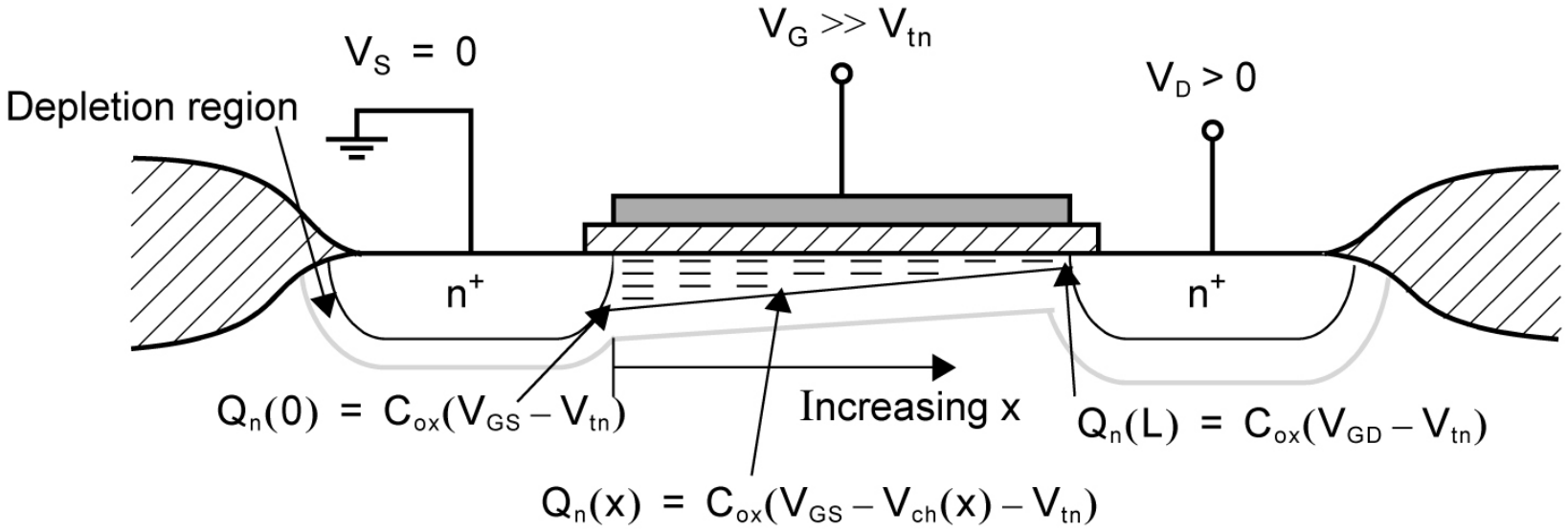


(*b*)

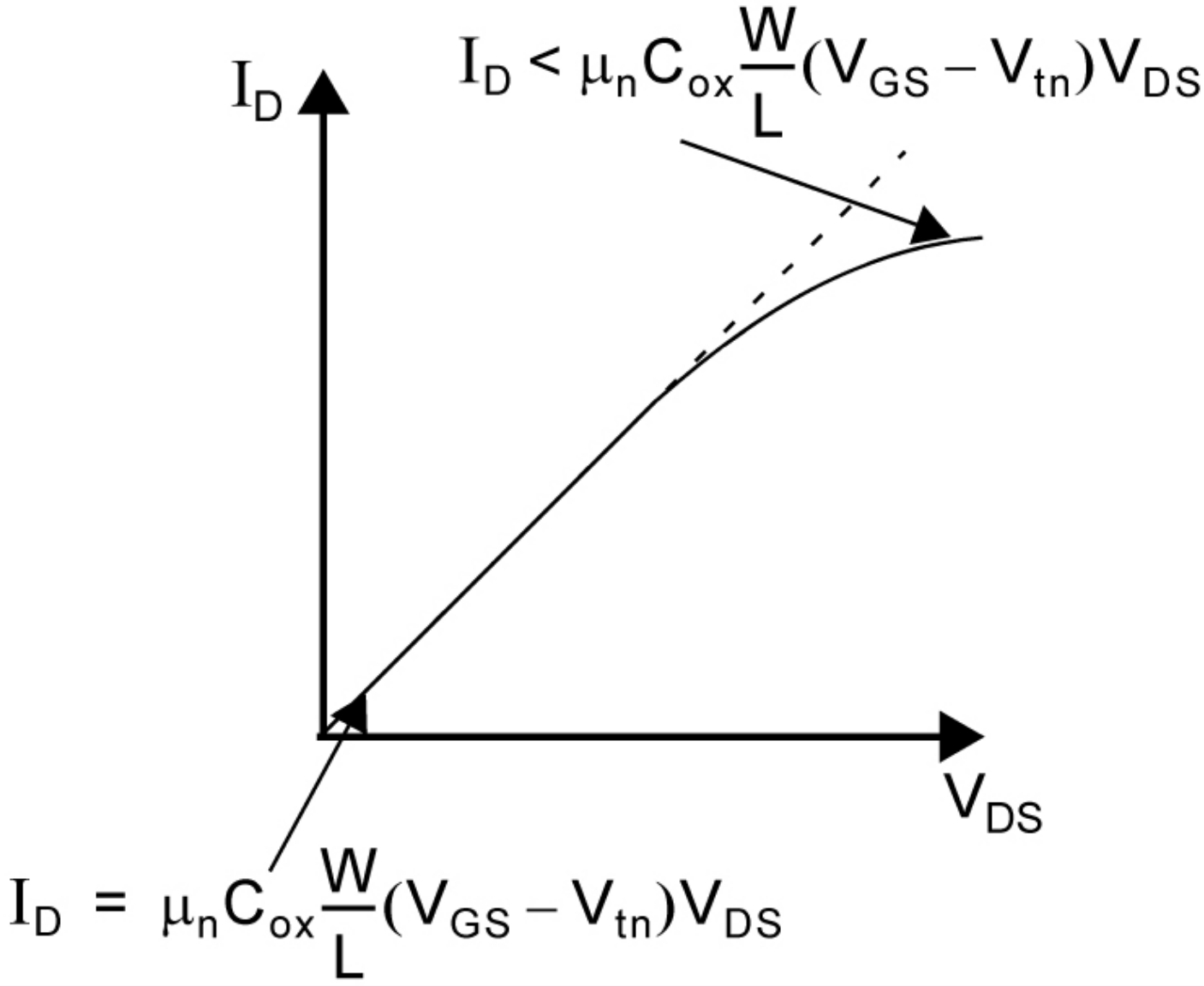
Resulting in an channel and current flow is possible depending on V_{DS}

Chapter 1 Figure 09

MOS operation II: triode(linear) region

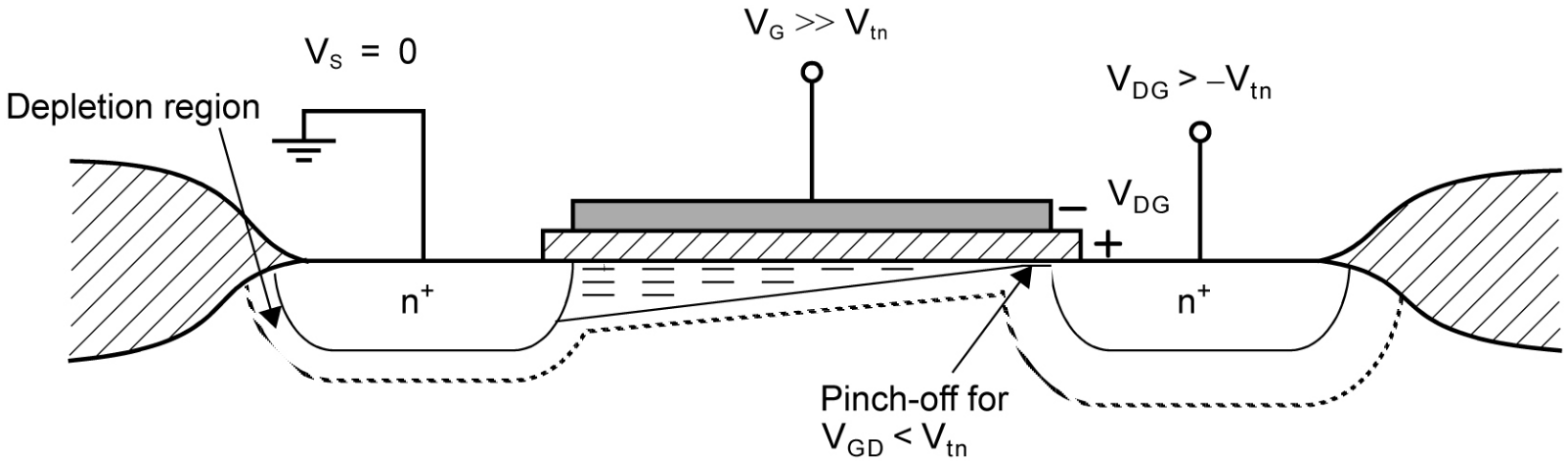


Chapter 1 Figure 11

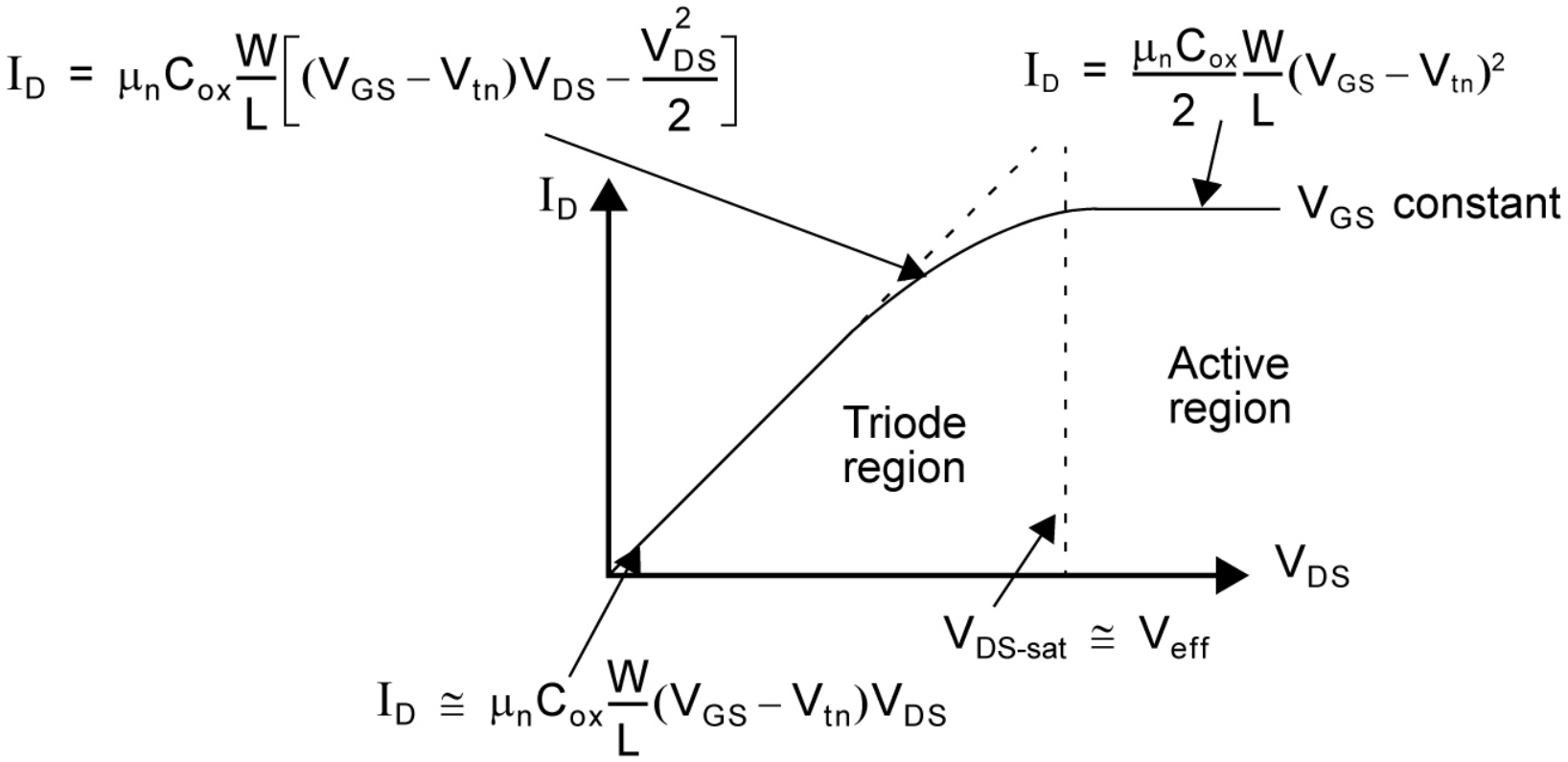


Chapter 1 Figure 12

MOS operation III: saturation (active) region



Chapter 1 Figure 13



Chapter 1 Figure 14

The threshold voltage

The threshold voltage of a transistor is not constant, but affected by the source-body voltage V_{SB}, this is called body effect.

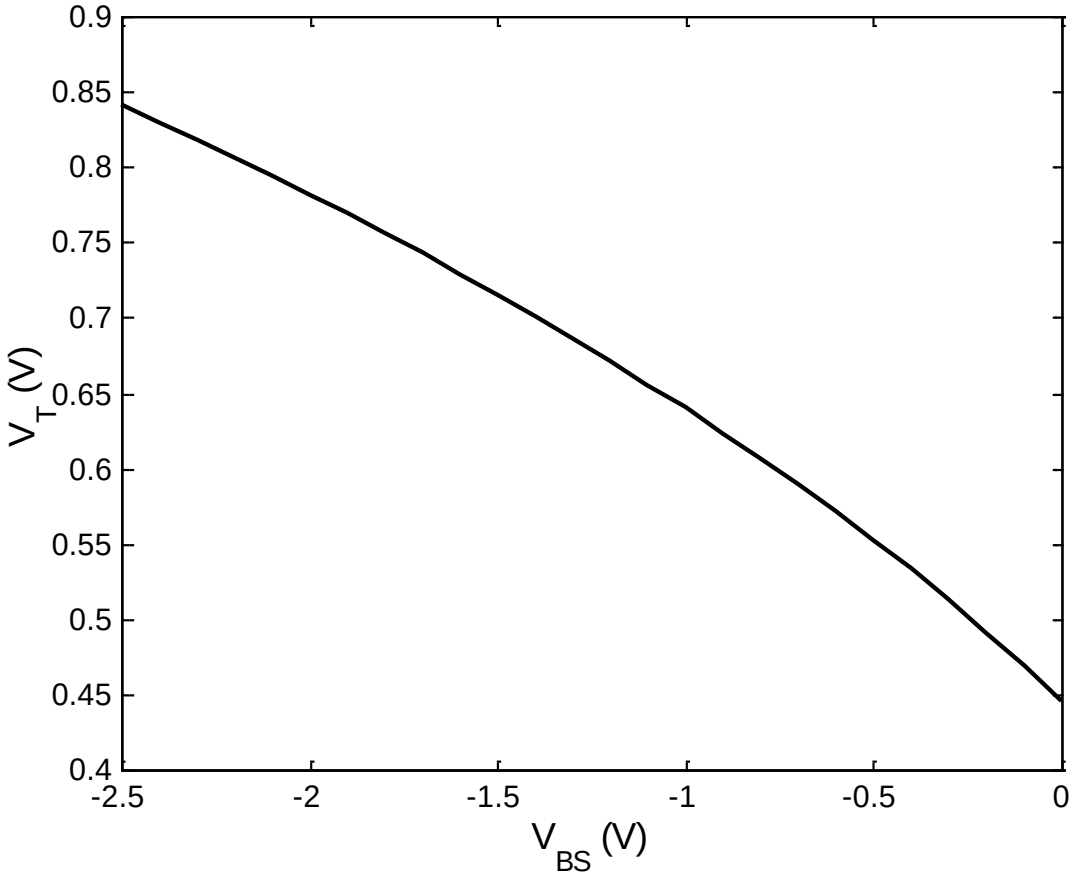
$$V_{tn} = V_{tn0} + \gamma(\sqrt{V_{SB} + |2\phi_F|} - \sqrt{|2\phi_F|})$$

where V_{tn0} is the threshold voltage with zero V_{SB} (source-to-body voltage), $\phi_F = (kT/q)\ln(N_A/n_i)$ is the Fermi potential of the body, and

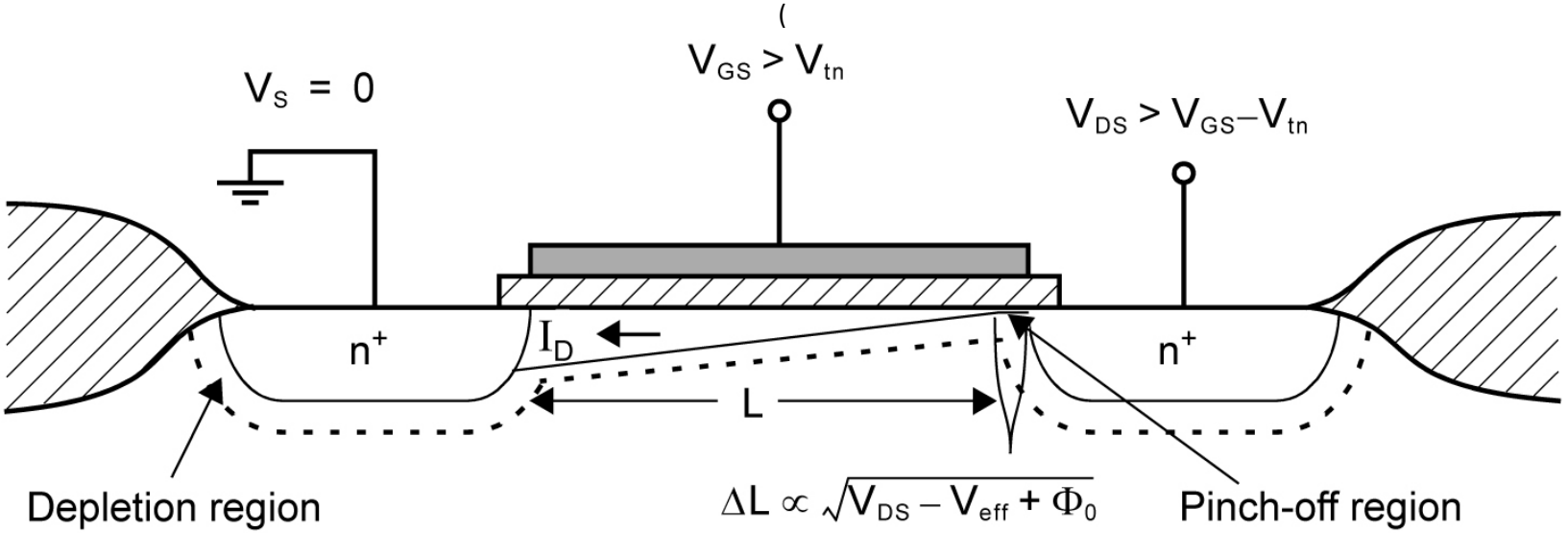
$$\gamma = \frac{\sqrt{2qN_AK_s\varepsilon_0}}{C_{ox}}$$

The factor γ is often called the *body-effect constant* and has units of $\sqrt{V}$. Notice that γ is proportional to $\sqrt{N_A}$,[12] so the body effect is larger for transistors in a well where typically the doping is higher than the substrate of the microcircuit.

Body effect on threshold voltage: an example



Channel length modulation



Chapter 1 Figure 15

$$I_D = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)(V_{GS} - V_{tn})^2[1 + \lambda(V_{DS} - V_{eff})] \qquad V_{eff} = V_{GS} - V_{tn}$$

$$\lambda = \frac{K_{ds}}{2L\sqrt{V_{DS} - V_{eff} + \emptyset_0}}$$

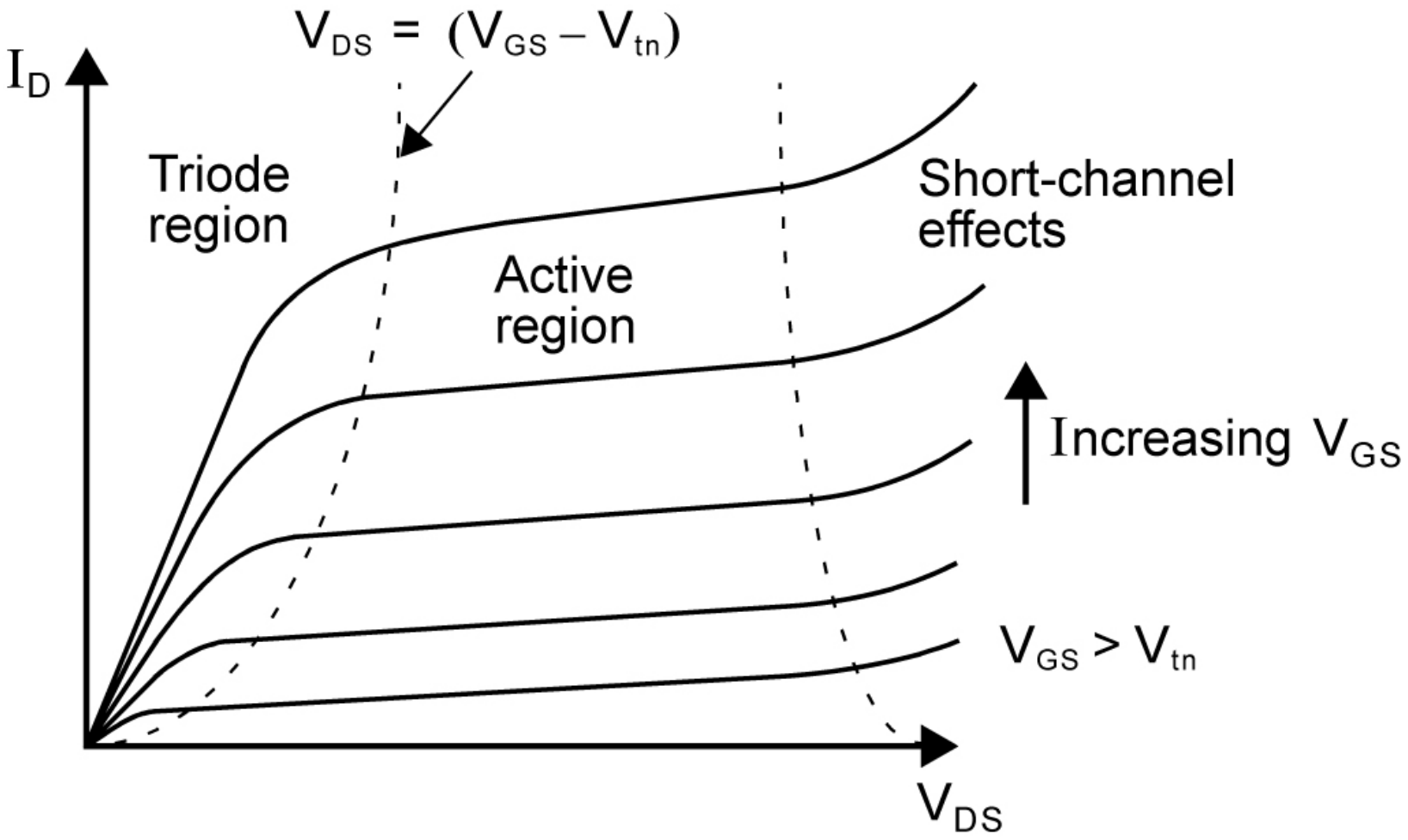
Note: inversely proportional to L

$$k_{ds} = \sqrt{\frac{2K_s\varepsilon_0}{qN_A}}$$

$$\Phi_0 = V_T \ln\left(\frac{N_A N_D}{n_i^2}\right)$$

Built in Junction potential

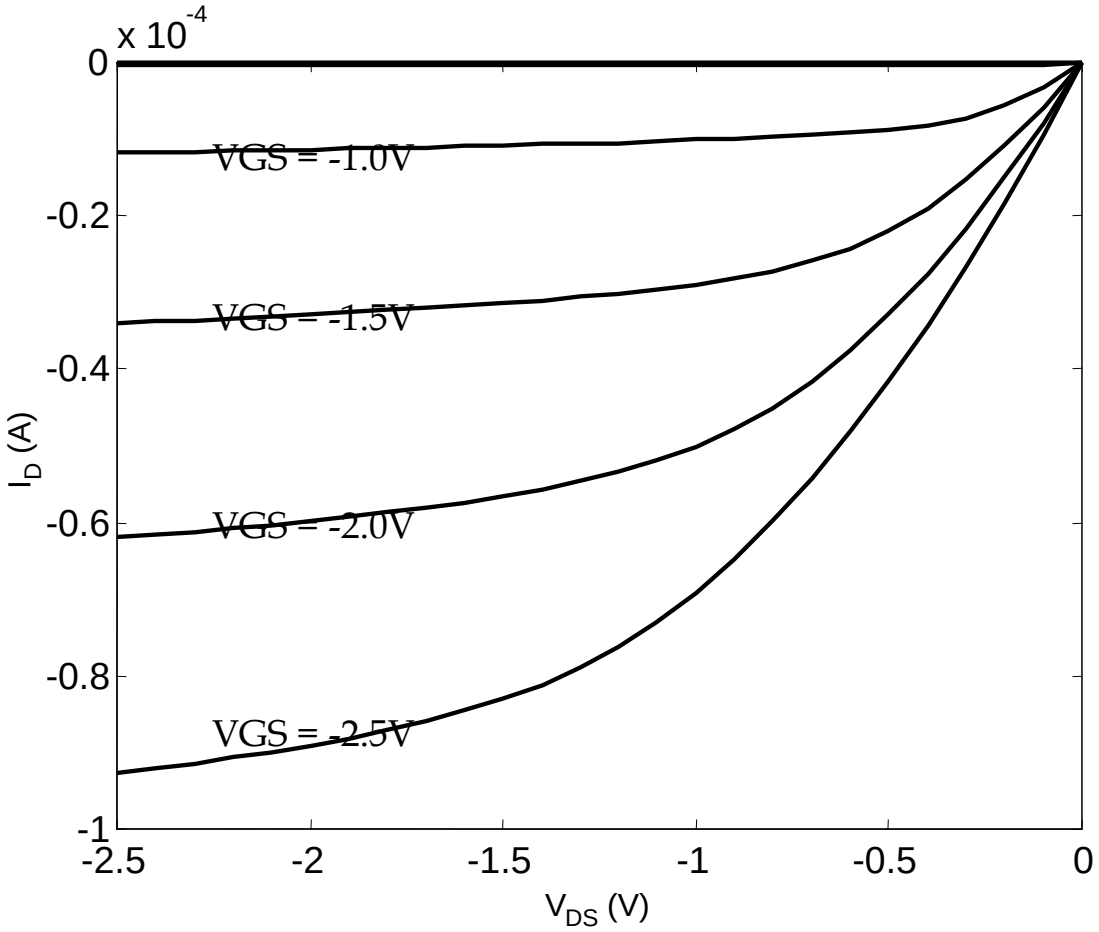
A summary of operation regions



Chapter 1 Figure 16

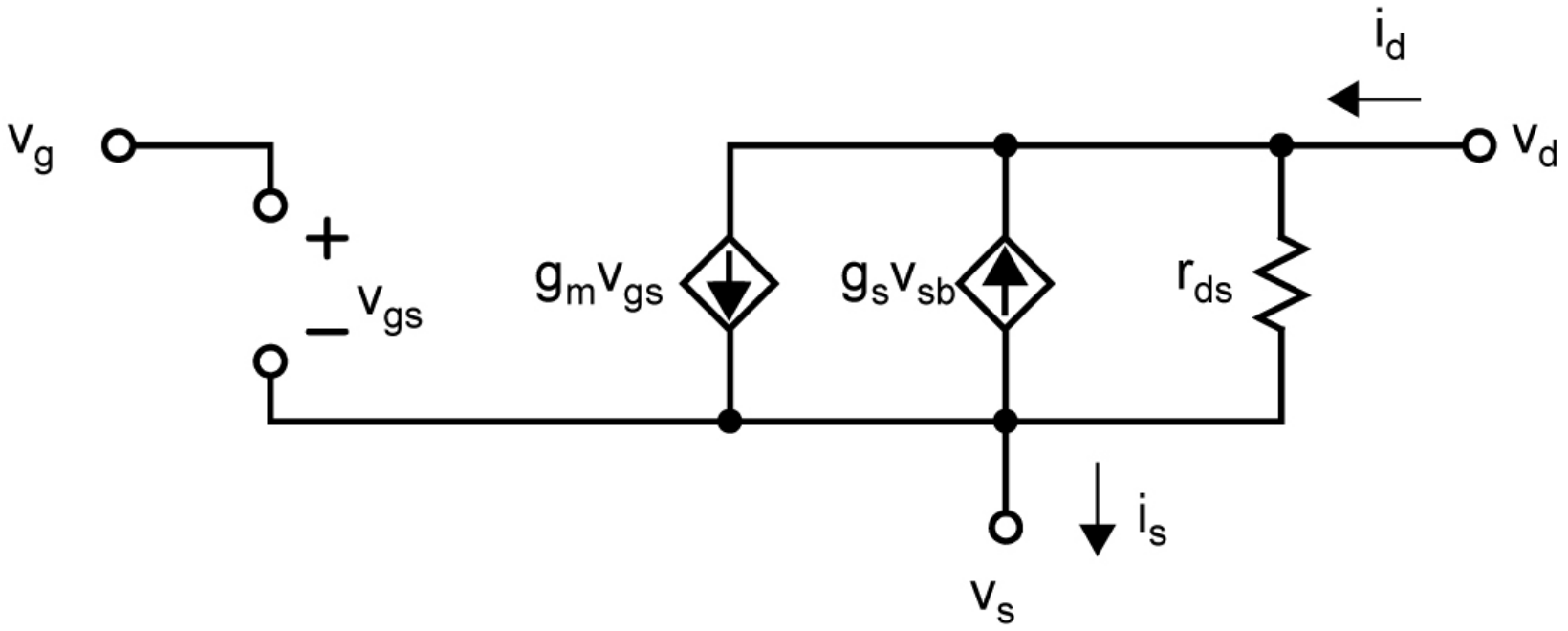
In analog amplifiers, MOS transistors are mostly used in active regions, but in digital circuits they often operate in both regions.

Operation of a PMOS transistor



Assume all variables negative!

Low frequency small-signal model (active)



Chapter 1 Figure 17

Low frequency small-signal model (active)

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{tn}) = \mu_n C_{ox}\frac{W}{L}V_{eff} \qquad V_{eff} \equiv V_{GS} - V_{tn}$$

$$g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D}$$

$$g_m = \frac{2I_D}{V_{eff}}$$

$$g_s = \frac{\gamma\, g_m}{2\sqrt{V_{SB} + |2\phi_F|}}$$

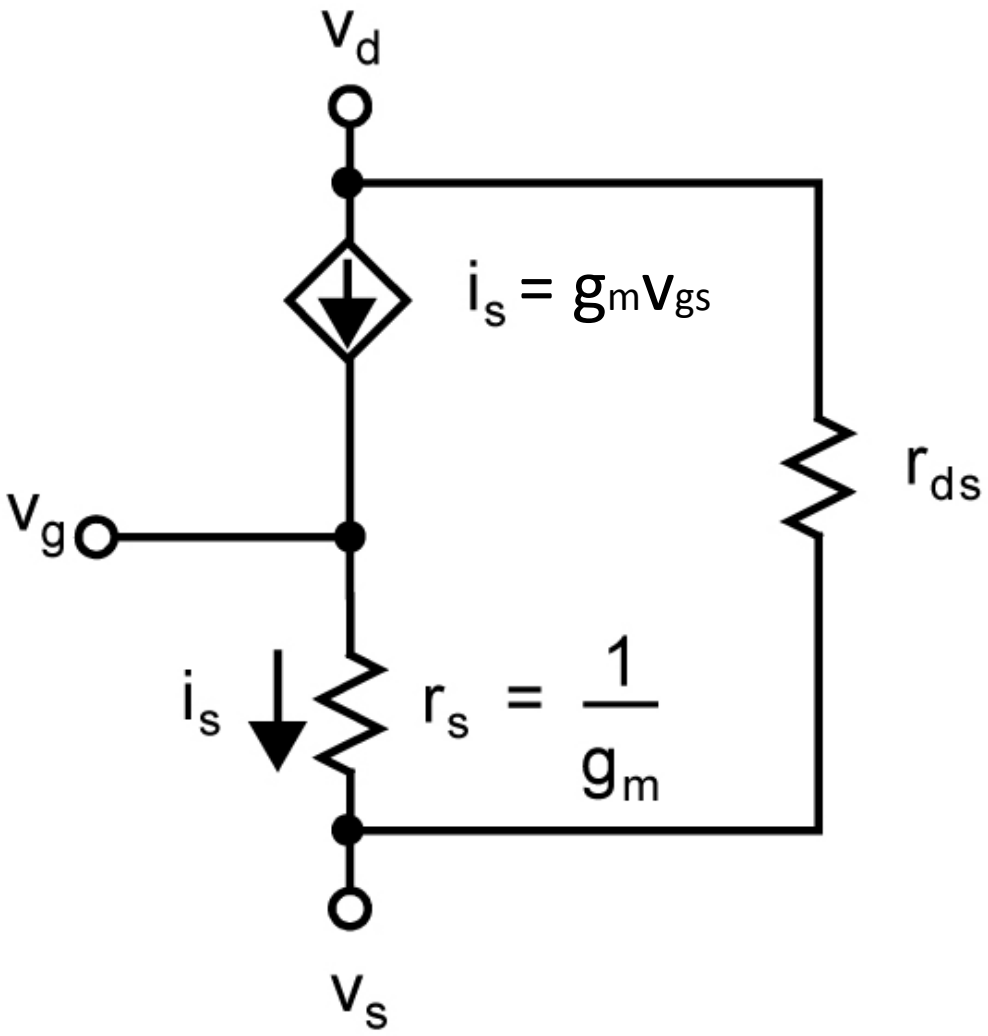
$$g_s = \frac{\partial I_D}{\partial V_{SB}} = \frac{\partial I_D}{\partial V_{tn}}\frac{\partial V_{tn}}{\partial V_{SB}} \qquad \frac{\partial I_D}{\partial V_{tn}} = -\mu_n C_{ox}\left(\frac{W}{l}\right)(V_{GS} - V_{tn}) = -g_m$$

$$V_{tn} = V_{tn0} + \gamma(\sqrt{V_{SB} + |2\phi_F|} - \sqrt{|2\phi_F|}) \qquad \frac{\partial V_{tn}}{\partial V_{SB}} = \frac{\gamma}{2\sqrt{V_{SB} + |2\phi_F|}}$$

$$\frac{1}{r_{ds}} = g_{ds} = \frac{\partial I_D}{\partial V_{DS}} = \lambda\left(\frac{\mu_n C_{ox}}{2}\right)\left(\frac{W}{L}\right)(V_{GS} - V_{tn})^2 = \lambda I_{D\text{-}sat} \cong \lambda I_D \qquad r_{ds} \cong \frac{1}{\lambda I_D}$$

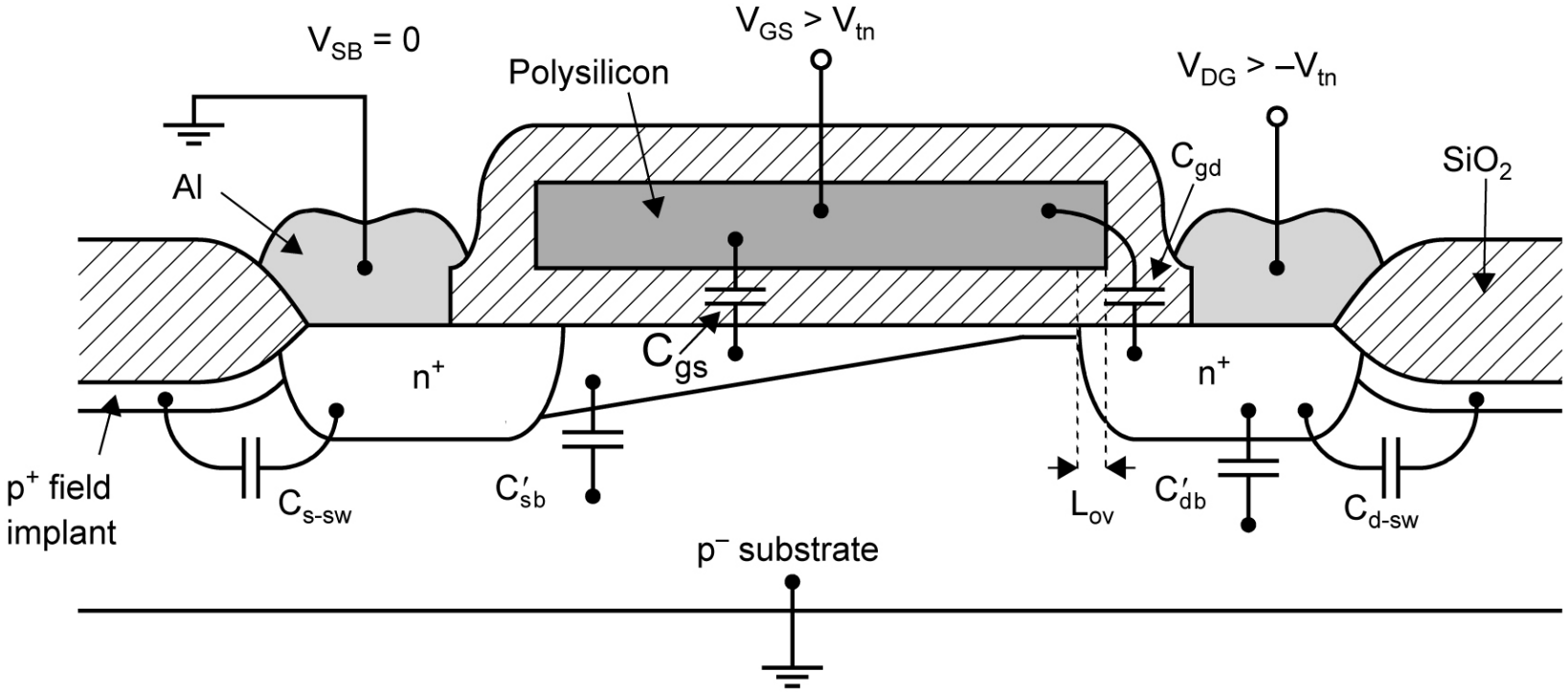
See page 25-28

An alternative low frequency small-signal model



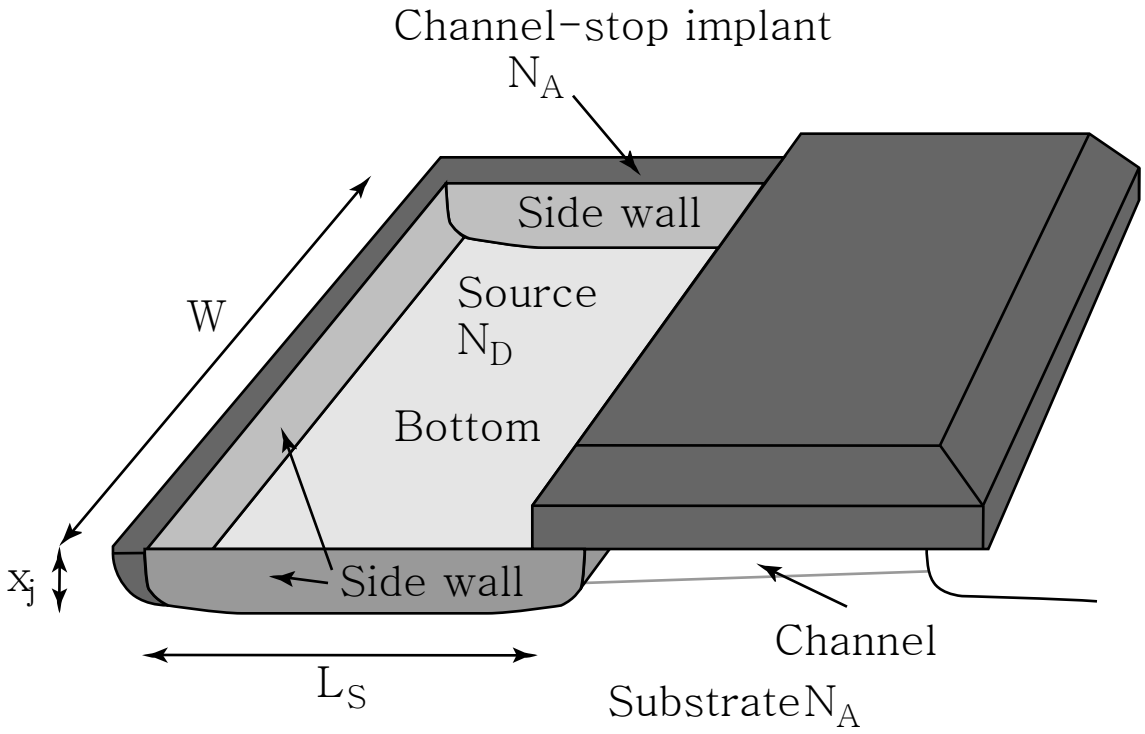
Chapter 1 Figure 20

Understanding parasitic capacitance (active)



Chapter 1 Figure 21

A little more detail on C_{db} and C_{sb}



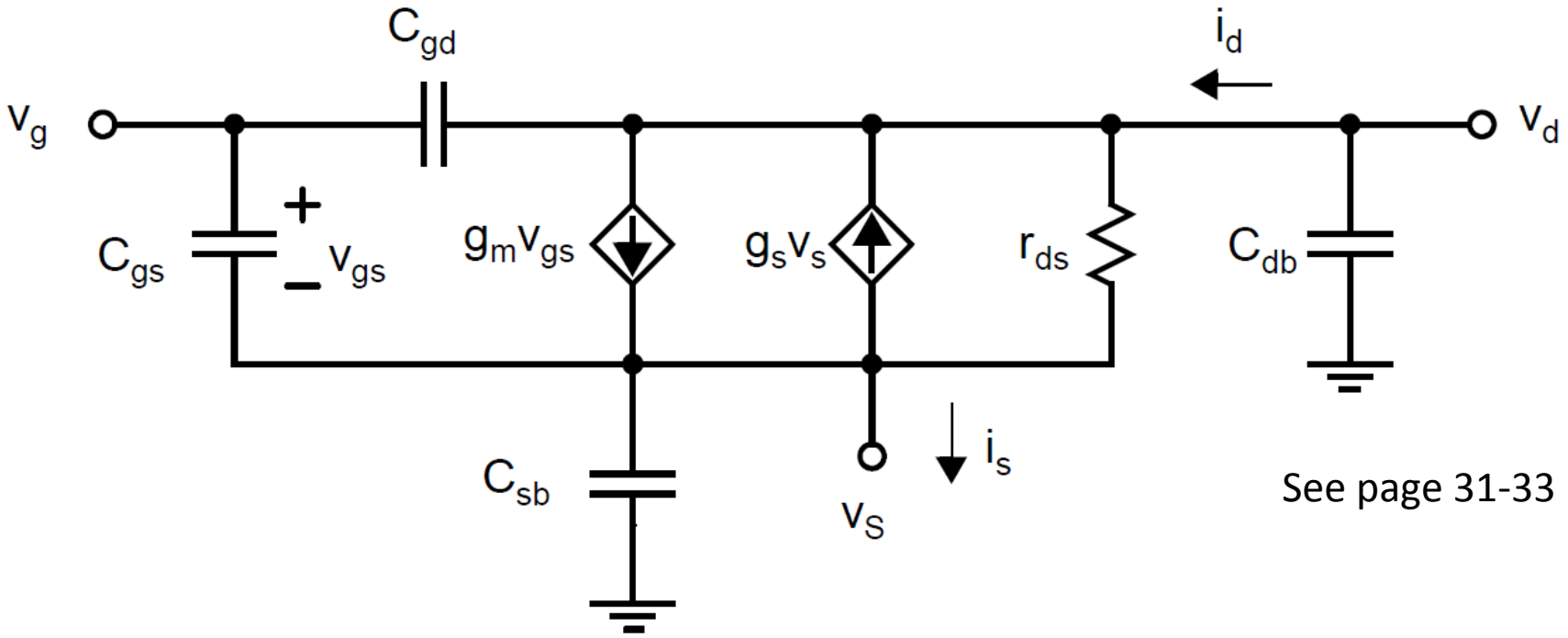
Junction capacitance per unit length

$$C_{diff} = C_{bottom} + C_{sw} = C_j \times AREA + C_{jsw} \times PERIMETER$$
$$= C_j L_S W + C_{jsw}(2L_S + W)$$

Junction capacitance per unit area

No channel side

High freqency small-signal model (active)



See page 31-33

$C_{gs} = \frac{2}{3}WLC_{ox} + C_{ov}$ Due to the change in channel charge by Vgs voltage

$C'_{sb} = (A_s + A_{ch})C_{js}$ Depletion capacitance and includes channel-body part

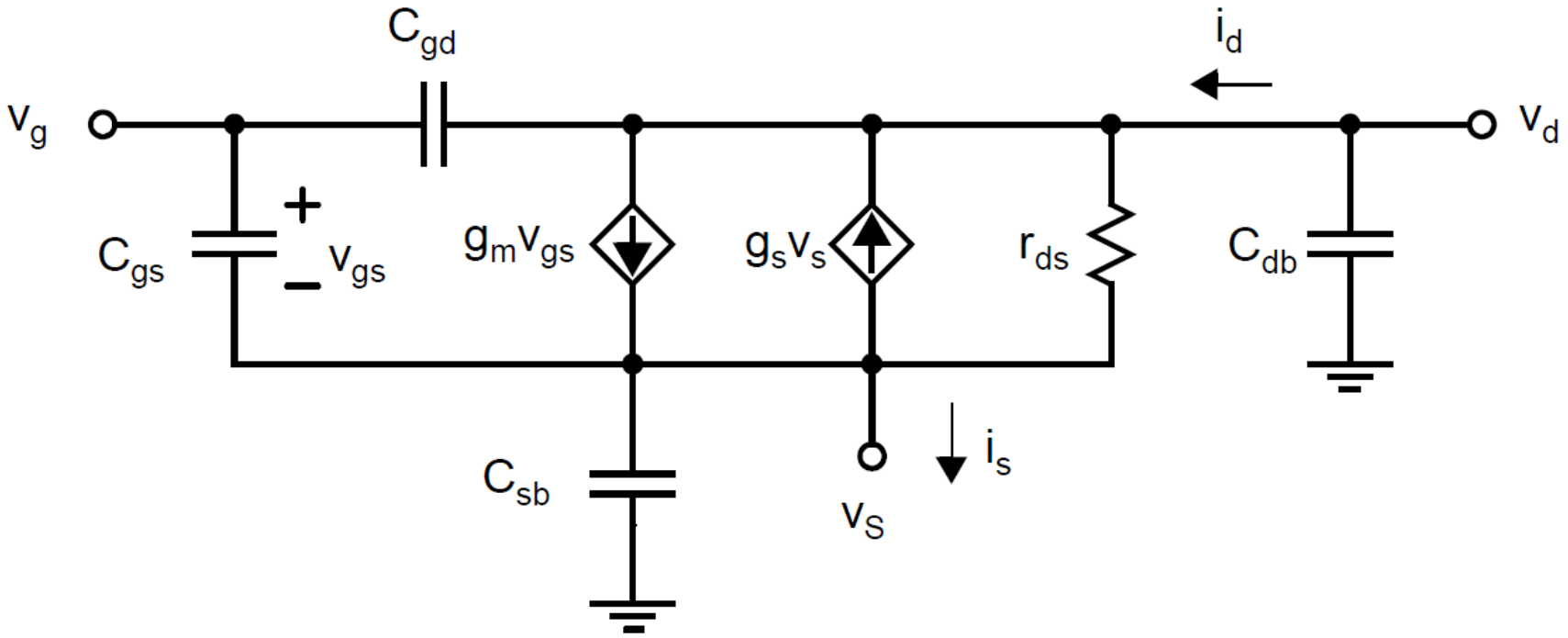
where A_s is the area of the source junction, A_{ch} is the area of the channel $C_{js} = \frac{C_{j0}}{\sqrt{1 + \frac{V_{SB}}{\Phi_0}}}$

$C_{s\text{-}sw} = P_s C_{j\text{-}sw}$

where P_s is the length of the perimeter of the source junction, excluding the side adjacent to the channel,

$C_{sb} = C'_{sb} + C_{s\text{-}sw}$

High freqency small-signal model (active)



Chapter 1 Figure 22

$C'_{db} = A_d C_{jd}$ Depletion capacitance but NOT includes channel-body part $C_{jd} = \dfrac{C_{j0}}{\sqrt{1 + \dfrac{V_{DB}}{\Phi_0}}}$

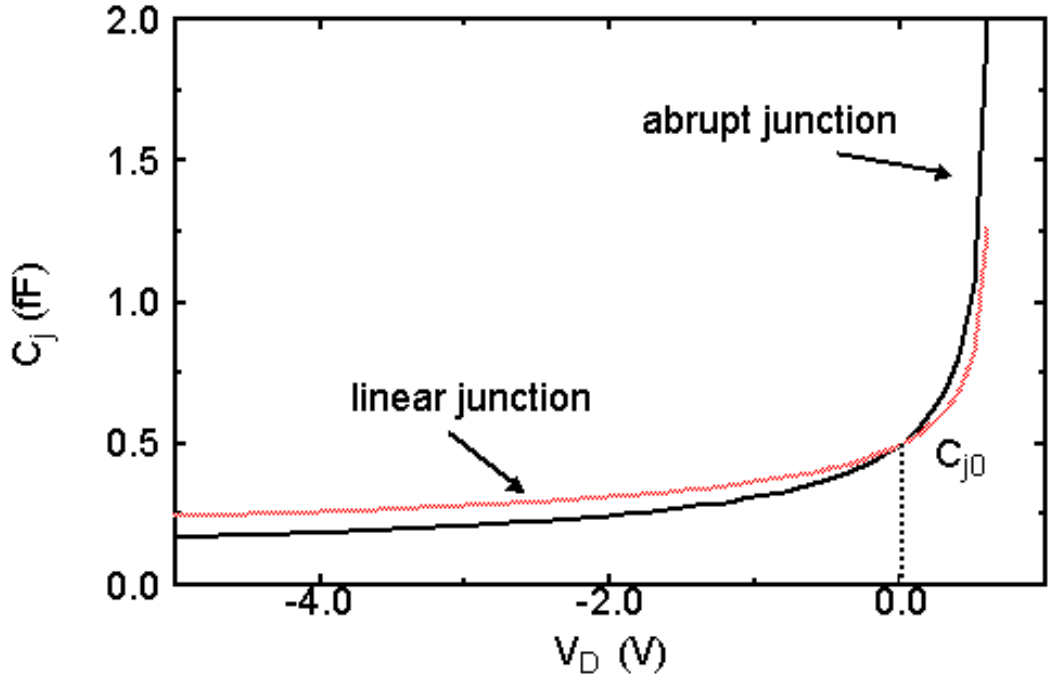
$C_{d\text{-}sw} = P_d C_{j\text{-}sw}$

$C_{db} = C'_{db} + C_{d\text{-}sw}$

$C_{gd} = C_{ox} W L_{ov}$

See page 31-33

Junction Capacitance



$$C_j = \frac{C_{j0}}{(1 - V_D/\phi_0)^m}$$

m = 0.5: abrupt junction
m = 0.33: linear junction

- Both C_j and C_{jsw} are non-linear and depends on the bias voltage.
- Keep large reverse-biased voltage for PN junction

A note on drain-body and source-body PN junctions

- In MOS transistors, both drain-body and source-body PN junctions have to be reverse-biased at all times.
- This means that for NMOS transistors, drain-body and source-body voltage must be larger than 0. Therefore, for NMOS, the body terminal is typically connected to the lowest power supply (such as Gnd or Vss).
- For PMOS, then the body terminal should be connected to the highest power supply (such as Vdd).

Two examples

Example 1.13 on page 33

An n-channel transistor is modelled as having the following capacitance parameters: $C_j = 2.4 \times 10^{-4}$ pF/(μm)^2, $C_{j\text{-}sw} = 2.0 \times 10^{-4}$ pF/μm, $C_{ox} = 1.9 \times 10^{-3}$pF/(μm)^2, $C_{ov} = 2.0 \times 10^{-4}$ pF/μm. Find the capacitances C_{gs}, C_{gd}, C_{db}, and C_{sb} for a transistor having $W = 100$ μm and $L = 2$ μm. Assume the source and drain junctions extend 4 μm beyond the gate.

$$A_s = A_d = 400\ (\mu m)^2$$

$$P_s = P_d = 108\ \mu m$$

$$C_{gs} = \left(\frac{2}{3}\right) WLC_{ox} + C_{ov} \times W = 0.27\ pF$$

$$C_{gd} = C_{ov} \times W = 0.02\ pF$$

$$C_{sb} = C_j(A_s + WL) + (C_{j\text{-}sw} \times P_s) = 0.17\ pF$$

$$C_{db} = (C_j \times A_d) + (C_{j\text{-}sw} \times P_d) = 0.12\ pF$$

Two examples

Derive the complete small-signal model for an NMOS transistor with I_{DS}=100μA, V_{SB}=0.15V, V_{DS}=0.6V. Device parameters are $2\phi_f = 0.65$, W=10μm, L=0.18μm, γ= 0.4$V^{1/2}$, $\mu_n C_{ox}$ = 200μA / V^2, λ = 0.4V^{-1}, t_{ox} = 40Å = 4nm, Ψ_0 = 0.69 V, C_{sb0} = C_{db0} = 9.3fF. Overlap capacitance from gate to source and gate to drain is 1fF. Assume C_{gb} =5fF.

$$g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D} = \sqrt{2\times 200\times 10^{-6}\times\frac{10}{0.18}\times 100\times 10^{-6}}\ A/V = 1.5\,mA/V$$

$$g_{mb} = \gamma\sqrt{\frac{\mu_n C_{ox}\frac{W}{L}I_D}{2(2\phi_f + V_{SB})}} = 0.4\sqrt{\frac{200\times 10^{-6}\times\frac{10}{0.18}\times 100\times 10^{-6}}{2\times(0.65+0.15)}}\ A/V = 333\,\mu A/V$$

$$r_o = \frac{1}{\lambda I_D} = \frac{1}{0.4\times 100\times 10^{-6}} = 25k\Omega$$

With V_{SB}=0.15V,we find $C_{sb} = \dfrac{C_{sb0}}{\left(1+\frac{V_{SB}}{\psi_0}\right)^{1/2}} = \dfrac{9.3}{\left(1+\frac{0.15}{0.69}\right)^{1/2}}\,fF = 8.4\,fF$

The voltage from drain to body is $V_{DB} = V_{DS} + V_{SB} = 0.75V$

Hence, $C_{db} = \dfrac{C_{db0}}{\left(1+\frac{V_{DB}}{\psi_0}\right)^{1/2}} = \dfrac{9.3}{\left(1+\frac{0.75}{0.69}\right)^{1/2}}\,fF = 6.4\,fF$

The oxide capacitance per unit area is

$$C_{ox} = \frac{\varepsilon_r\varepsilon_{SiO_2}}{t_{ox}} = \frac{3.9\times 8.854\times 10^{-14}\ F/cm}{40\times 10^{-10}\ m} \sim 8.6\ fF/(\mu m)^2$$

The intrinsic portion of the gate source capacitance is

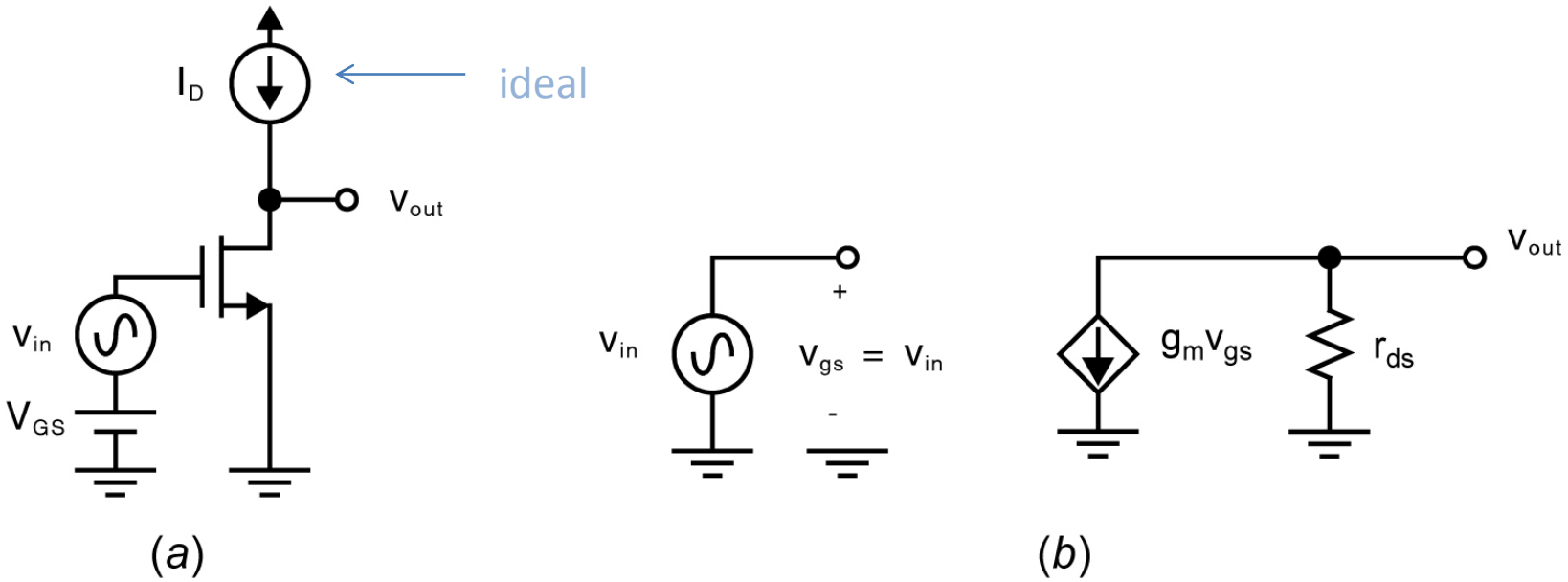
$$C_{gs} = \frac{2}{3}\times 10\times 0.18\times 8.6\,fF \sim 10\,fF$$

Analog Figure-of-Merit

With so many small-signal parameters, it is useful to have a single number that captures key aspects of transistor performance.

Two such figure of merits are intrinsic gain (low frequency performance) and intrinsic speed (high frequency performance).

Analog Figure-of-Merit I



Chapter 1 Figure 26

$$A_i = \left|\frac{v_{out}}{v_{in}}\right| = g_m r_{ds} \cong \frac{2I_D}{V_{eff}} \cdot \frac{1}{\lambda I_D} = \frac{2}{\lambda V_{eff}}$$

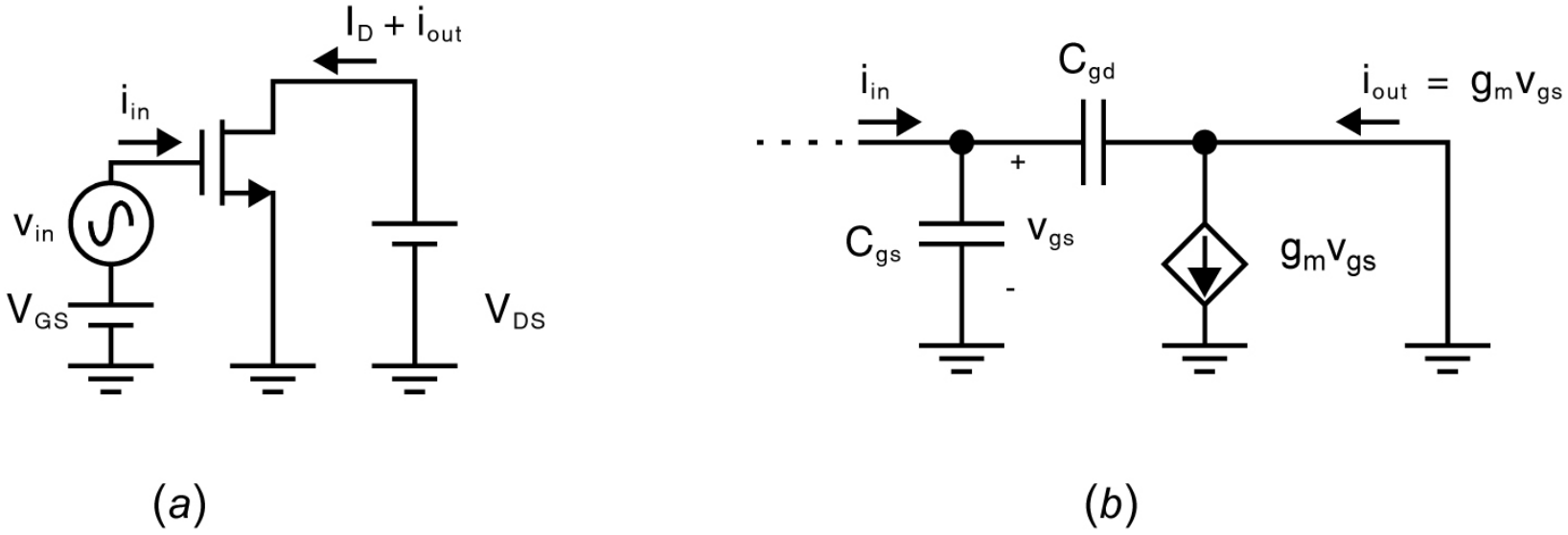
Two important general conclusions on analog design:

1. To maximize DC or low frequency gain, transistor needs to have small V_{eff}
2. Intrinsic gain is maximized when gate length L is large so that λ is small

Analog Figure-of-Merit II

The unit-gain frequency of a transistor, ft, is to provide a measure of the maximum operating frequency at which a transistor is useful (used as a measure of intrinsic speed).

The UGF is defined as the maximum frequency at which the amplitude of the output small-signal current |Iout| is still larger than |Iin|.



Chapter 1 Figure 27

$$f_t \approx \frac{g_m}{2\pi(C_{gs}+C_{gd})} \approx \frac{\mu_n C_{ox}(W/L)V_{eff}}{2\pi C_{ox}W(2/3)L} = \frac{3\mu_n V_{eff}}{4\pi L^2} \qquad \text{assuming } C_{gs} \gg C_{gd}$$

Analog Figure-of-Merit II

As with intrinsic gain, some important fundamental conclusions about analog design can be drawn:

1. For operation at high-speed, devices parasitic capacitances should be minimized, which implies minimizing device gate length L.
2. Speed is maximized by biasing with high values of Veff.

Note that there requirements are in direct conflict with those for maximum gain.

2^{nd}-order effects affecting transistor operation

Subthreshold leakage current (when Vgs < Vt)

Velocity saturation

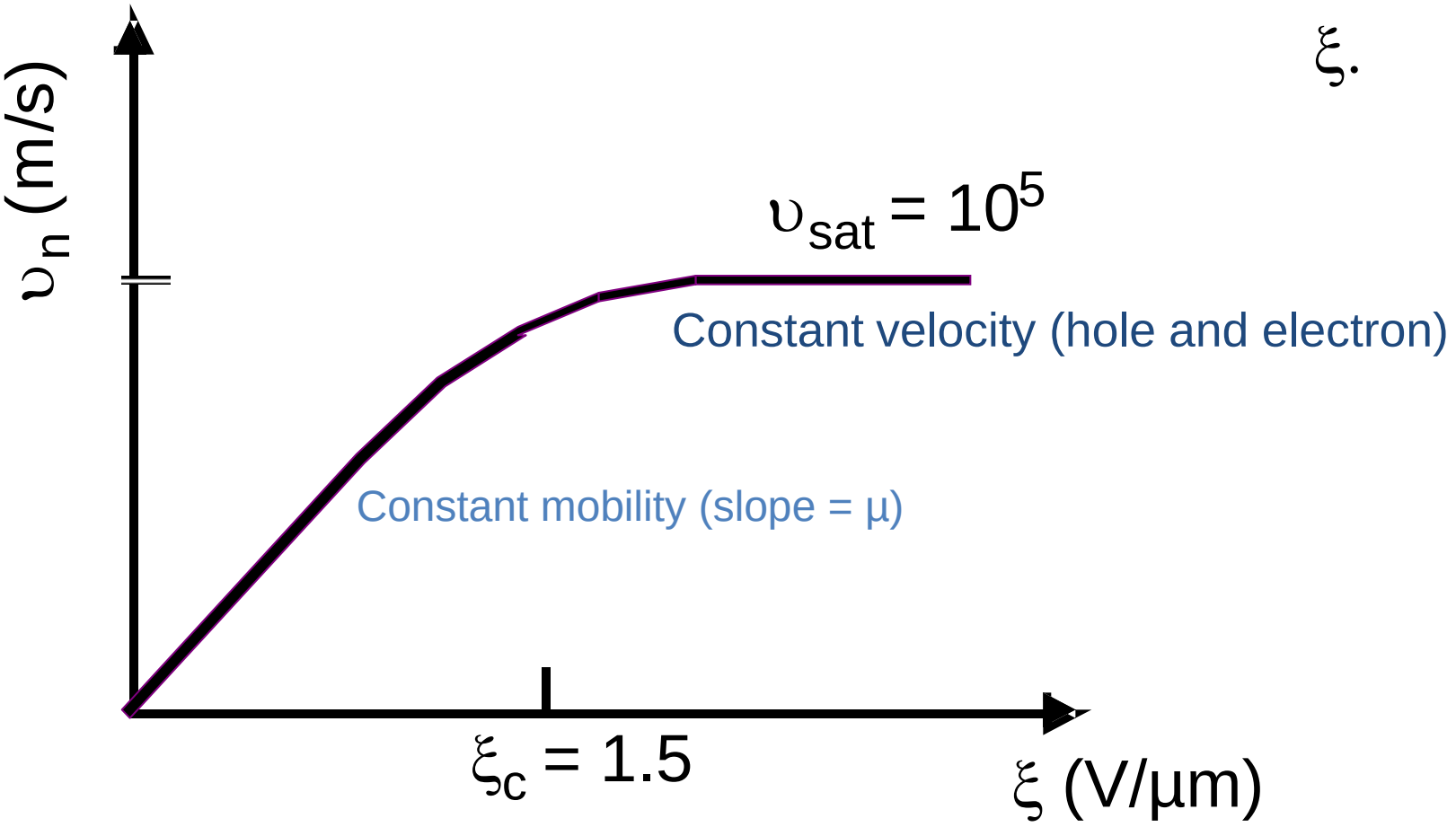
Parasitic resistances

Junction leakage current

Velocity Saturation

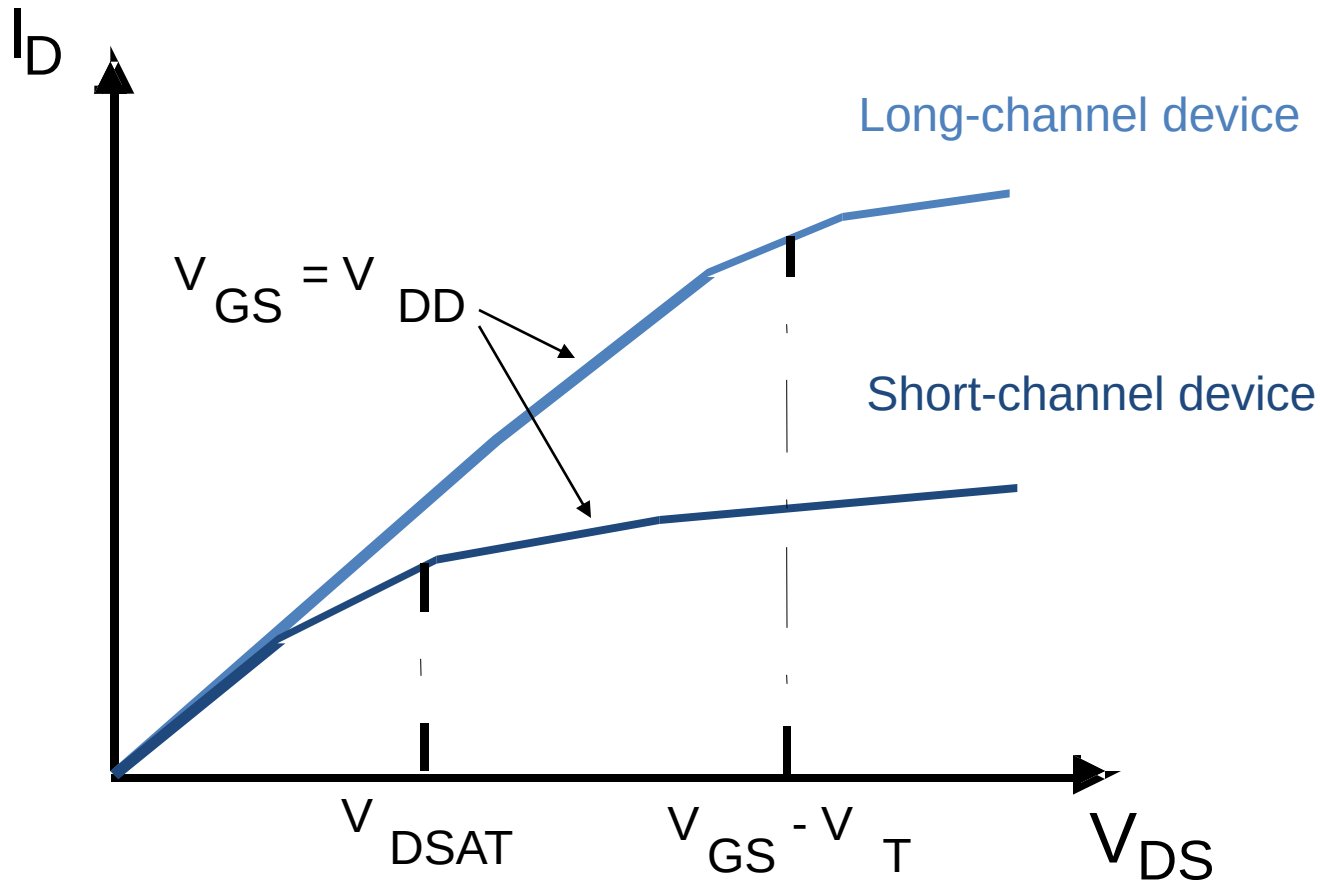
The critical field at which saturation occurs depends on both doping levels and vertical electrical field. Typically 1 to 5v/um for
(2V across 0.25µm channel).

ξ.

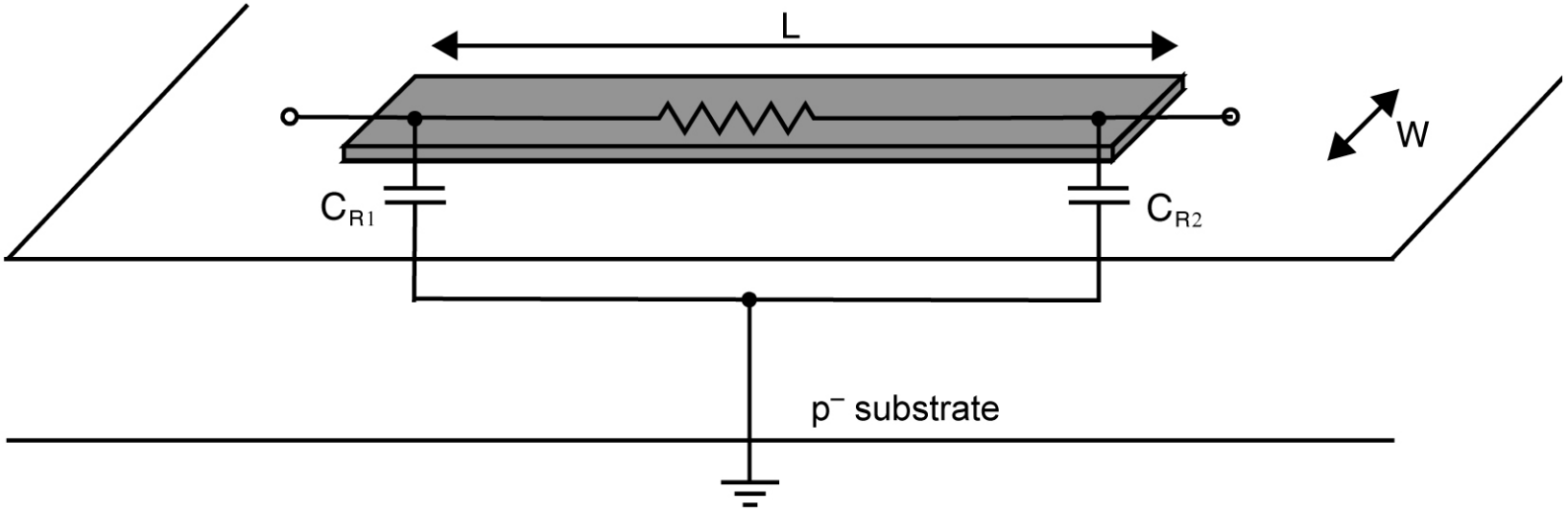


Perspective

When increasing the V_{DS}, the electrical field in the channel ultimately reaches the critical value and the carriers at the drain become velocity saturated (gives a early saturation at V_{DSAT}).



Resistor in an IC



Chapter 1 Figure 34

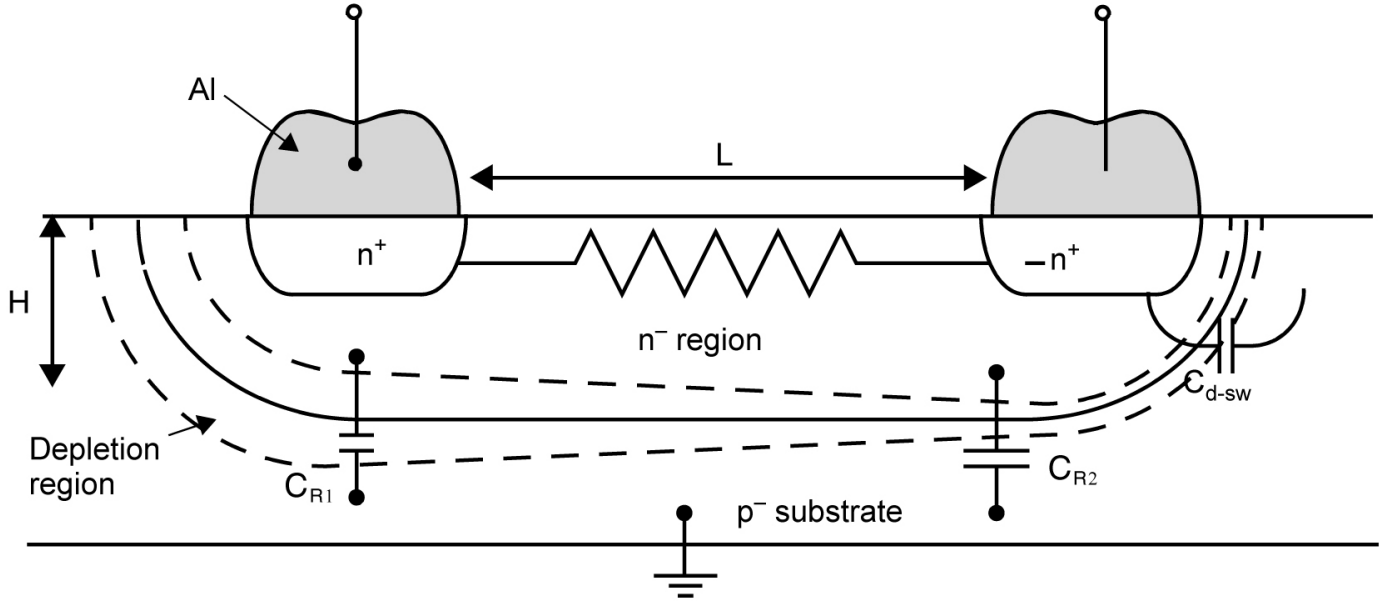
The simplest realization of an integrated circuit resistor is a strip of conductive material above the silicon substrate.

The conductivity of the material is characterized by sheet resistance, $R_{\square}$

$$R = R_{\square}\left(\frac{L}{W}\right)$$

It has parasitic capacitance in the model.

Resistor in an IC



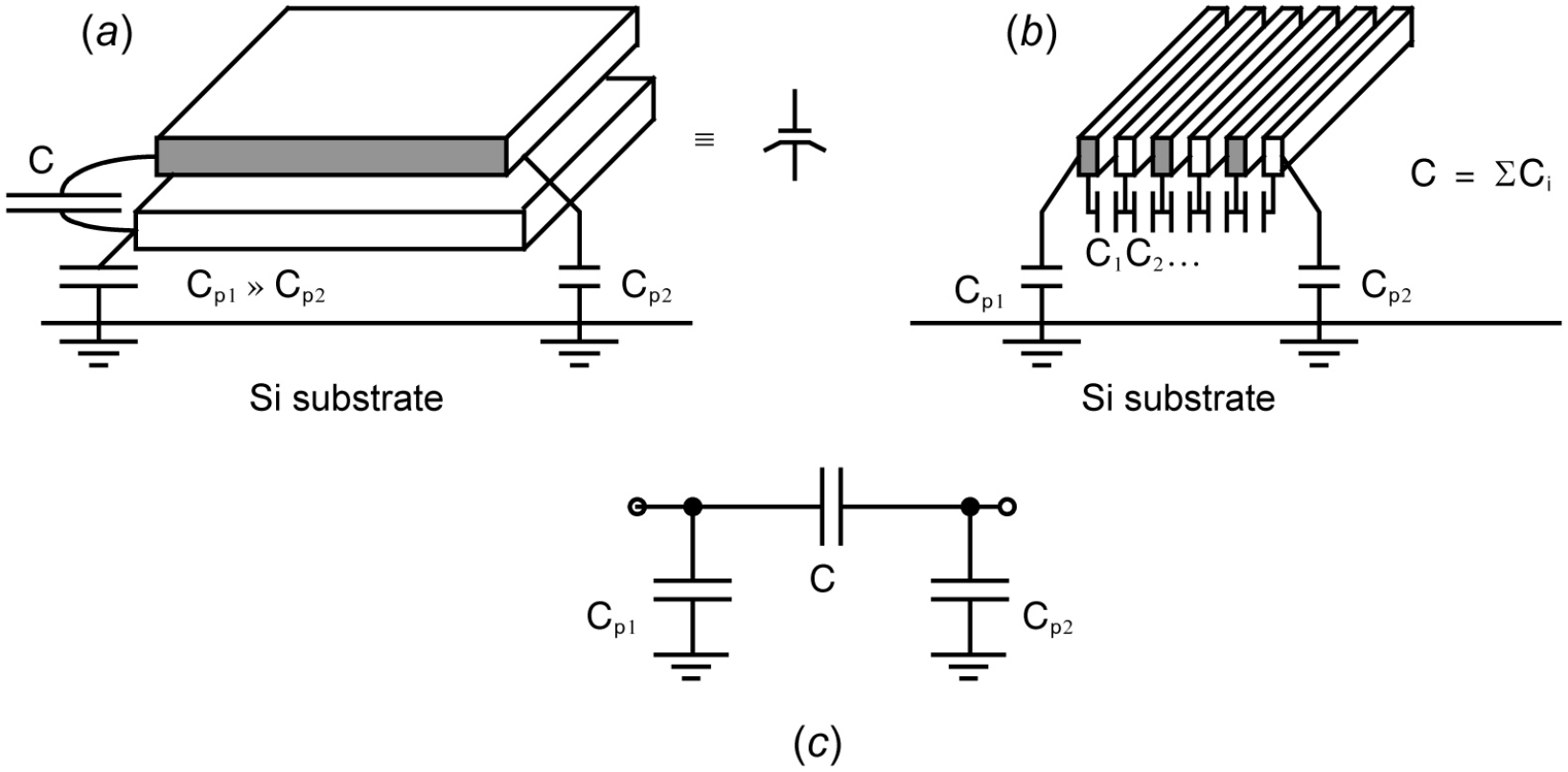
Chapter 1 Figure 35

A lightly-doped nwell with contacts at both ends may be used a resistor.

The model still apply for this type of resistor. However, it has complex dependency on temperature and the voltage across it, making it varying and nonlinear.

Another method to implement a resistor is to operate a transistor in triode region, where the resistance is mostly modulated by Vgs.

Capacitor in an IC



Chapter 1 Figure 37

For implementation of a linear capacitor, metal-to-metal is a popular approach.

$$C \cong \frac{\varepsilon_{ox} A}{t_{ox}}$$

where t_{ox} is the spacing between plates (on the order of 0.1 - 10 μm), ε_{ox} is the permittivity of the insulator between plates (often silicon dioxide, for which $\varepsilon_{ox} \cong 3.9\varepsilon_0$), and A is the area of the plate.

Other approaches, such as poly-to-poly, poly-to-diffusion, are possible.

SPICE model parameters

Table 1.2 Important SPICE parameters for modelling diodes.

SPICE Parameter	Model Constant	Brief Description	Typical Value
IS	I_S	Transport saturation current	10^{-17} A
RS	R_d	Series resistance	30 Ω
TT	τ_T	Diode transit time	12 ps
CJ	C_{j0}	Capacitance at 0-V bias	0.01 pF
MJ	m_j	Diode grading coefficient exponent	0.5
PB	Φ_0	Built-in diode contact potential	0.9 V

Chapter 1 Table 02

Table 1.3 A reasonable set of Level 2 or 3 MOS parameters for a typical 0.8-μm technology.

SPICE Parameter	Model Constant	Brief Description	Typical Value
VTO	V_{tn}:V_{tp}	Transistor threshold voltage (in V)	0.8:–0.9
UO	μ_n:μ_p	Carrier mobility in bulk (in $cm^2/V \cdot s$)	500:175
TOX	t_{ox}	Thickness of gate oxide (in m)	1.8×10^{-8}
LD	L_D	Lateral diffusion of junction under gate (in m)	6×10^{-8}
GAMMA	γ	Body-effect parameter	0.5: 0.8
NSUB	N_A:N_D	The substrate doping (in cm^{-3})	3×10^{16}:7.5×10^{16}
PHI	$\|2\phi_F\|$	Surface inversion potential (in V)	0.7
PB	Φ_0	Built-in contact potential of junction to bulk (in V)	0.9
CJ	C_{j0}	Junction-depletion capacitance at 0-V bias (in F/m^2)	2.5×10^{-4}:4.0×10^{-4}
CJSW	$C_{j\text{-}sw0}$	Sidewall capacitance at 0-V bias (in F/m)	2.0×10^{-10}:2.8×10^{-10}
MJ	m_j	Bulk-to-junction exponent (grading coefficient)	0.5
MJSW	$m_{j\text{-}sw}$	Sidewall-to-junction exponent (grading coefficient)	0.3

Chapter 1 Table 03

Table 1.4 A summary of modern SPICE model formats.

SPICE Model	Main strengths compared with previous device models
BSIM3	Improved modeling of moderate inversion, and the geometry-dependence of device parameters. This also marked a return to a more physics-based model as opposed to the preceding highly empirical models.
EKV	Relates terminal currents and voltages with unified equations that cover all modes of transistor operation, hence avoiding discontinuities at transitions between, for example, weak and strong inversion. Also handles geometry-dependent device parameters.
BSIM4	Improved modeling of leakage currents and short-channel effects, noise, and parasitic resistance in the MOSFET terminals, as well as continued improvements in capturing the geometry-dependence of device parameters.
PSP	Improved modeling of noise and the many short-channel and layout-dependent effects now dominant in nanoscale CMOS devices. Particular effort was made to accurately model nonlinearities, which requires accuracy in the high-order derivatives of the transistor's voltage–current relationships.

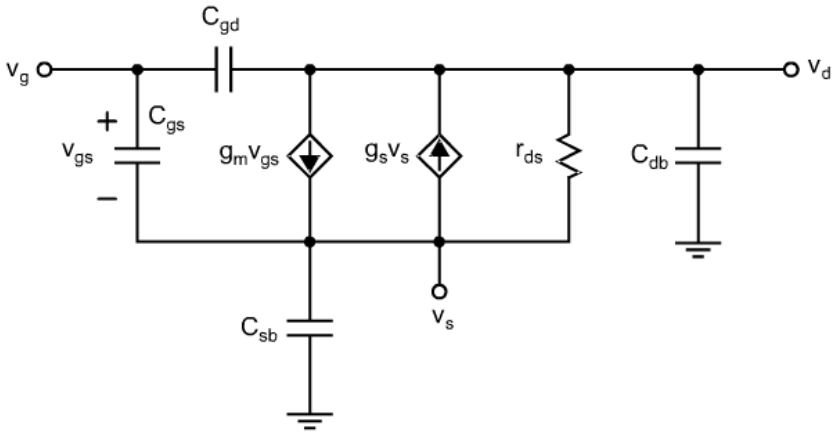
Chapter 1 Table 04

Table 1.5 MOSFET parameters representative of various CMOS technologies and used for rough hand calculations in this text.

	0.8 μm		0.35 μm		0.18 μm		45 nm	
Technology	**NMOS**	**PMOS**	**NMOS**	**PMOS**	**NMOS**	**PMOS**	**NMOS**	**PMOS**
μC_{ox} ($\mu A/V^2$)	92	30	190	55	270	70	280	70
V_{t0} (V)	0.80	–0.90	0.57	–0.71	0.45	–0.45	0.45	–0.45
$\lambda \cdot L$ ($\mu m/V$)	0.12	0.08	0.16	0.16	0.08	0.08	0.10	0.15
C_{ox} ($fF/\mu m^2$)	1.8	1.8	4.5	4.5	8.5	8.5	25	25
t_{ox} (nm)	18	18	8	8	5	5	1.2	1.2
n	1.5	1.5	1.8	1.7	1.6	1.7	1.85	1.85
θ (1/V)	0.06	0.135	1.5	1.0	1.7	1.0	2.3	2.0
m	1.0	1.0	1.8	1.8	1.6	2.4	3.0	3.0
$C_{ov}/W = L_{ov}C_{ox}$ ($fF/\mu m$)	0.20	0.20	0.20	0.20	0.35	0.35	0.50	0.50
$C_{db}/W \approx C_{sb}/W$ ($fF/\mu m$)	0.50	0.80	0.75	1.10	0.50	0.55	0.45	0.50

Chapter 1 Table 05

Summary



$g_m = \mu_n C_{ox}\left(\frac{W}{L}\right)V_{eff}$	$g_m = \sqrt{2\mu_n C_{ox}(W/L)I_D}$
$g_m = \frac{2I_D}{V_{eff}}$	$g_s = \frac{\gamma g_m}{2\sqrt{V_{SB} + \lvert 2\phi_F \rvert}}$
$r_{ds} = \frac{1}{\lambda I_{D\text{-}sat}} \cong \frac{1}{\lambda I_D}$	$g_s \cong 0.2 g_m$
$\lambda = \frac{k_{rds}}{2L\sqrt{V_{DS} - V_{eff} + \Phi_0}}$	$k_{rds} = \sqrt{\frac{2K_s\varepsilon_0}{qN_A}}$
$C_{gs} = \frac{2}{3}WLC_{ox} + WL_{ov}C_{ox}$	$C_{gd} = WL_{ov}C_{ox}$

$C_{sb} = (A_s + WL)C_{js} + P_s C_{j\text{-}sw}$	$C_{js} = \frac{C_{j0}}{\sqrt{1 + V_{SB}/\Phi_0}}$
$C_{db} = A_d C_{jd} + P_d C_{j\text{-}sw}$	$C_{jd} = \frac{C_{j0}}{\sqrt{1 + V_{DB}/\Phi_0}}$